A Built-In Self-Test Approach for the Embedded Resistor Array in TI MSP430 Microcontrollers

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Abstract. In this paper, we propose a built-in self-test (BIST) for the resistor array in an embedded analog configurable circuit (EACC) that is present in the Texas Instruments® MSP430 microcontrollers family. The EACC is formed also by an Operational Amplifier (OA) and interconnection resources. We focus in the resistor array test due to this section establishes the feedback path for the embedded OAs and set the gain value for the EACC closed-loop configurations. The test establishes, through very simple measurements, which combinations of the resistor ladder are available for the user by using only the resources embedded in the microcontroller. The experimental results show that the BIST proposed presents a very good repeatability in the measurements with very low dispersion, for one chip, for a sample of chips and under different temperature conditions. The error in the measurements, evaluated using a higher precision voltmeter, is also low. These results show that the BIST proposed is useful for testing the functionality of the resistor array in the EACC under test using a simple strategy at a very low cost.

Keywords: built-in self-test; mixed signal testing; embedded analog test; microcontroller test.

1 Introduction

Embedded analog and digital configurable sections included in modern microcontrollers (μCs) facilitate the chip adaptation to different environments. They offer a broad pool of resources for performing a wide variety of operations, like signal conditioning, analog to digital conversion and digital signal processing.

Testing an embedded analog configurable circuit (EACC) in a μC is a significant challenge. In addition to the well known problems related to analog-circuits testing, other particular characteristics of EACCs make difficult the implementation of effective test strategies. One of these is the strong interaction between the analog and digital portions that often requires accessing the analog sections through complex digital interfaces. By other way, the low controllability or observability makes difficult the stimulus application and response evaluation. Finally, the usually high

number of possible configurations that presents an EACC implies many different circuits to be tested.

A relatively low number of researchers have addressed the test of configurable analog circuits. In [1], [2], is presented an online testing strategy for continuous-time field programmable analog arrays (FPAAs). In [3], [4], [5], well-known off-line techniques such as oscillation-based test (OBT) and transient analysis method (TRAM) have been successfully applied to FPAAs for testing interconnection resources and basic building blocks. However, in the aforementioned papers the test strategies do not consider the use of resources that are present in embedded systems, like the CPU or analog to digital converters (ADCs).

In this paper, we propose a built-in self-test (BIST) strategy for an EACC available in the MSP430 μCs family from Texas Instruments®. The EACC is composed by operational amplifiers (OAs), interconnection resources and resistor arrays. Particularly, we focus in the resistor array test due to this section establishes the feedback path for the embedded OAs and set the gain value for closed-loop configurations.

The BIST could be used in different scenarios, for instance as part of a broader software-based BIST (SW-BIST) strategy that tests the functionality of all the EACC components. In SW-BIST, a programmable core (or a microprocessor core) functions as pattern generator and response analyzer to test other components embedded in the system [6], [7]. Within this context, the BIST could be also used as a low-cost self-test procedure for maintenance purposes. By other way, when an application demands fault tolerance, the BIST strategy could provide a low-cost off-line test periodically applied for establishing the gain that can be effectively programmed by the processor core, before a reconfiguration procedure.

Our strategy employs only the hardware and software resources of the μC. This characteristic is the main contribution of this paper, but it is also the main challenge, because the resources of the μC limit the testing signals able to be used.

2 TI MSP430 Overview

The MSP430 μC is based on a 16-bits RISC CPU. It presents RAM and FLASH memories (for data and program respectively), timer modules, dedicated communication controllers, and an ADC, among others resources. The block diagram of the system, obtained from the datasheet provided by the vendor is depicted in Fig.1. This figure shows the CUT and highlighted the blocks used by the BIST proposed here.

The EACCs in the MSP430 are the so-called OA modules (OAM0 and OAM1 in Fig. 1). Fig. 2 depicts the schematic diagram of one of these modules. As it is shown in this figure, an OA (OAx), several analog multiplexers, a resistor ladder and other resources compose each OAM. The multiplexers driven by the signal *Mode Selection* establish different OAM configurations, called by the manufacturer as “Modes” (Table 1). N-input MUX and P-input MUX select different input signal paths. Internal connections allow the OAM to provide the front end for the ADC (ADC10 in Fig. 1) [8].

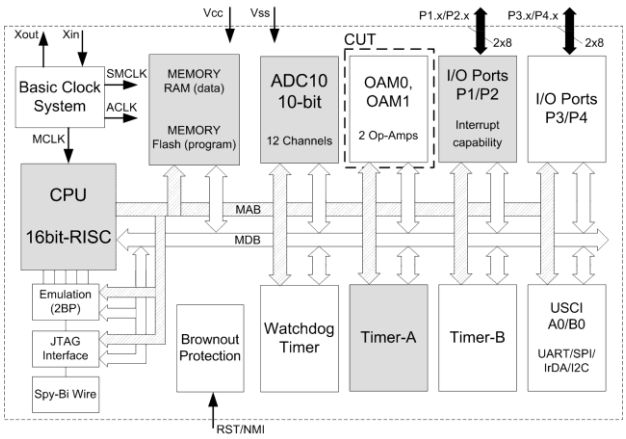

Fig. 1. Block diagram of the microcontroller chosen as a case study.

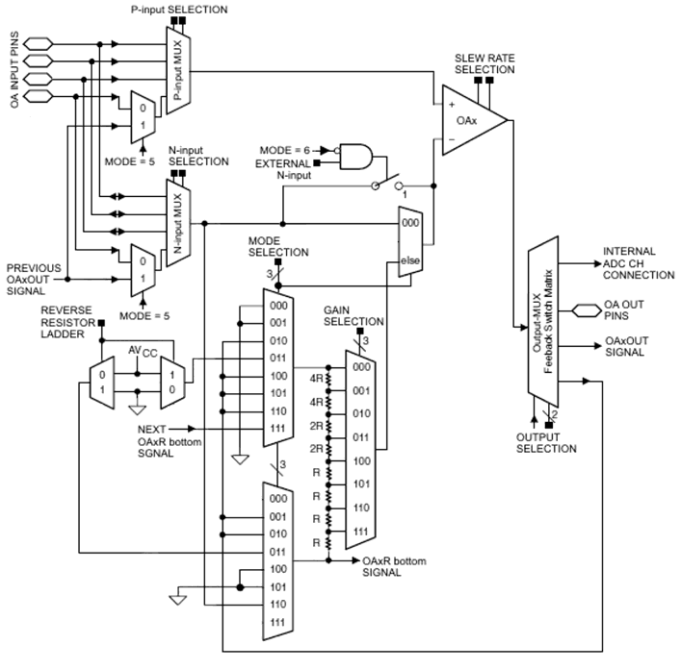

Fig. 2. Schematic diagram of OA module.

Table 1. OAM Modes.

Mode Selection value	OAM mode
000	0 – General purpose OA
001	1 - Unity gain buffer for three-OA differential amplifier
010	2 - Unity gain buffer
011	3 – Comparator
100	4 - Non-inverting PGA[1]
101	5 - Cascaded non-inverting PGA
110	6 - Inverting PGA
111	7 - Differential amplifier

For each OAM, a programmable resistor ladder sets the gain in the modes that present amplification (4, 5, 6 and 7) by the use of the multiplexer driven by *Gain Selection* signal. Additionally, it establishes a programmable reference voltage level when the OAM is configured as a comparator (mode 3). The OAM configuration is register-based and can be reprogrammed by the user at runtime. A detailed description of the module is out of the scope of this work and is provided by the vendor in [9].

3 Resistor Ladder Test

Our test approach establishes which combinations of the resistor ladder in the OAM are available for the user by using only the resources embedded in the μC: the processor core and the 10 bits ADC. The processor executes an embedded test routine that sequentially programs a number of configurations for the resistor array, acquires data and performs calculations. Fig. 3 shows the OAM setup configured by the test routine, valid for the two available modules OAM0 and OAM1 in the specific device adopted as case study (MSP430F2274).

We propose to take advantage of some characteristics of mode 3 (*Mode Selection* = 011) for accessing to the internal nodes of the resistor array. In this mode, the OA behaves as comparator with a programmable threshold voltage selected by the *Gain Selection* bits. This reference voltage, provide by the resistor array, is available at the OA input V_{in-} by programming the MUX which is connected to this input. The set of the *External N-input* signal makes the internal V_{in-} value externally available in a pin.

In this way, we are able to measure all the values for the programmable reference using the ADC. To this end, the test routine configures a route from the pin to an ADC channel (CH2 for OA0 and CH5 for OA1) and acquires the programmable reference voltage value for both OAMs.

[1] PGA: Programmable Gain Amplifier

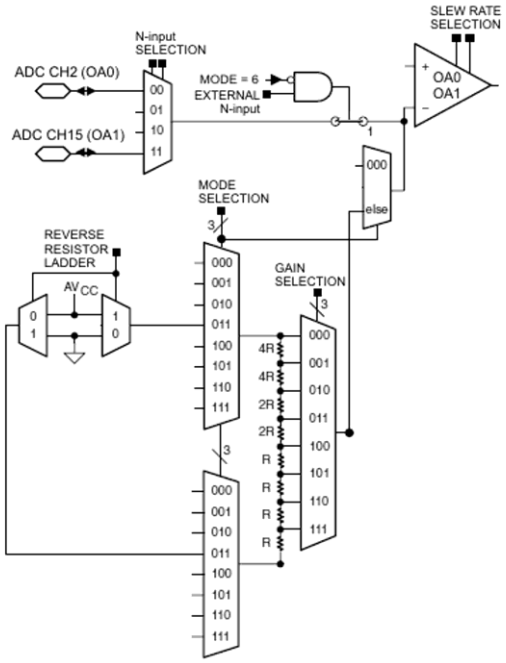

Fig. 3. Setup of OAM for testing the resistor array (valid for OAM0 and OAM1).

For the sake of clarity, Fig. 4 shows a simplified diagram of the resistor ladder. The multiplexer driven by *Gain Selection* establishes the point of the resistor ladder to be connected to V_{in}-. This point divides the resistor ladder in two, R_{top} and R_{bottom}. The signal *Reverse Resistor Ladder* (*RRL*) establishes the reference voltage (analog ground or analog power supply AV_{CC}) at the top of R_{top} and at the bottom of R_{bottom}. The programmable reference voltage value (V_{ref}) available at V_{in}- is:

$$V_{ref} = (R_{bottom}/(R_{bottom} + R_{top})) \cdot AV_{CC}, \quad RRL = 1. \tag{1}$$

$$V_{ref} = (R_{top}/(R_{bottom} + R_{top})) \cdot AV_{CC}, \quad RRL = 0. \tag{2}$$

For instance, with the values of *Gain Selection* = 3 and *RRL* = 1, R_{top} is equal to 10R and R_{bottom} is equal to 6R, where R is a unit resistance value. The V_{ref} value available for testing in this example is $3/8AV_{CC}$.

From the measurement of V_{ref} and the value AV_{CC}, the test routine establishes all values of the programmed relations of R_{top} and R_{bottom} and checks if they are within limits specified by the user. In this way, the routine indirectly tests the correctness of the gain values for the other modes due to the resistance ratios determine them.

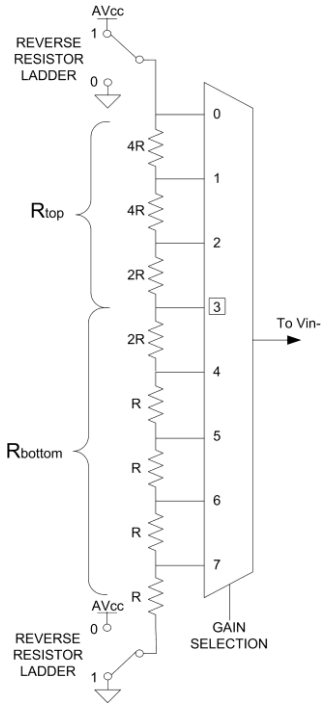

Fig. 4. Simplified diagram of the resistor ladder.

The test routine does not test the V_{ref} value for all the combinations of the signals *Gain Selection* and *RRL*. Instead it tests the right operation of both multiplexers (driven by the above mentioned signals). Table 2 shows the selected configurations of the two signals, labeled as "Test Condition". We chose the test conditions in the way shown in the table in order to minimize the effect of the noise level in the measurements.

Table 2. Test conditions.

Test Condition	Configuration	Ideal value for V_{ref} [AVcc units]
1	RRL = 1; Gain selection = 001	0.75
2	RRL = 1; Gain selection = 010	0.5
3	RRL = 0; Gain selection = 011	0.625
4	RRL = 0; Gain selection = 100	0.75
5	RRL = 0; Gain selection = 101	0.812
6	RRL = 0; Gain selection = 110	0.875
7	RRL = 0; Gain selection = 111	0.937

4 Experimental Results

The test routine has been written in C language using IAR Embedded Workbench for TI MSP430 C/C++ compiler and amounts to about 790 bytes of program memory in the μC. The experiments were performed in a TI eZ430-RF2500, a complete USB-based MSP430 wireless development kit that provides the necessary hardware to evaluate the MSP430F2274 μC. For the device chosen in this work, the total routine execution time is 4.4ms with a CPU clock (Master clock, MCLK) of 1MHz. The μC is supplied with 3.628V (AV_{CC} value) and it is operated at free-air temperature.

As it was mentioned in Section 3, the test procedure performs all the measurements using the internal ADC, which is a 10 bits successive-approximation converter. The total unadjusted error determines the overall deviation in the digital code delivered by the ADC channel from an ideal conversion. This error includes offset, gain, and nonlinearity errors in its calculation. The μC datasheet quotes a typical value of ±2LSB for the total unadjusted error with a maximum of ±5LSB. We consider here ±5LSB (±17.733mV for our test conditions) as the maximum measurement error.

The first test routine evaluation is the measurement repeatability. For doing this task, the test procedure is repeated 100 times for each test condition. Table 3 summarizes the results of the first test routine evaluation. It presents the mean value as a measure of central tendency, and the maximum and the minimum values as a measure of dispersion for V_{ref} in each test condition.

Table 3. Experimental results.

Parameter	Test condition	Min	Mean	Max	Measured
Voltage level available at the resistor ladder OA0 V_{ref} [AV_{CC} units]	1	0,749	0,749	0,75	0,747
	2	0,5	0,5	0,501	0,498
	3	0,625	0,625	0,626	0,623
	4	0,749	0,75	0,75	0,748
	5	0,812	0,813	0,814	0,81
	6	0,874	0,875	0,875	0,873
	7	0,936	0,937	0,938	0,936
Voltage level available at the resistor ladder OA1 V_{ref} [AV_{CC} units]	1	0,748	0,749	0,75	0,747
	2	0,499	0,5	0,501	0,497
	3	0,624	0,625	0,626	0,623
	4	0,749	0,75	0,751	0,748
	5	0,812	0,813	0,814	0,811
	6	0,874	0,874	0,875	0,874
	7	0,936	0,937	0,938	0,936

The data shows that all measurements present a very low dispersion around the mean value and are very similar for both OAMs. The maximum deviation is 0.2% (related to the mean value) for Test Condition 2 in both OA0 and OA1, and it is always below the above-mentioned maximum error. By other way, the mean values are very close to the ideal values reported in Table 2.

The second test routine evaluation contrasts the measurements made by the BIST with the performed ones using an Agilent 34401A multimeter with a resolution of 6 ½

digits. This contrast is possible because V_{ref} is available at a pin, as was explained in Section 3. The test environment is the same of the first test routine evaluation. The experimental results are also reported in Table 3, in the column Measured parameter. For this evaluation, the data show a very good correlation between the values obtained by the test routine and the experimental ones, being the maximum relative error 0.804%, for OA1 under Test Condition 2.

Table 4. Experimental results under different temperature conditions (First part).

OAM	Test condition	V_{ref} [V_{CC} units] 40ºC			V_{ref} [V_{CC} units] 60ºC		
		Min	Mean	Max	Min	Mean	Max
	1	0,748	0,749	0,75	0,748	0,749	0,75
	2	0,499	0,5	0,5	0,499	0,5	0,501
	3	0,625	0,625	0,626	0,625	0,625	0,626
OA0	4	0,749	0,75	0,75	0,749	0,75	0,75
	5	0,812	0,813	0,813	0,812	0,813	0,814
	6	0,873	0,874	0,875	0,873	0,874	0,875
	7	0,936	0,937	0,938	0,936	0,937	0,938
	1	0,748	0,749	0,75	0,748	0,749	0,75
	2	0,499	0,5	0,501	0,499	0,50	0,501
	3	0,624	0,625	0,626	0,624	0,625	0,626
OA1	4	0,749	0,75	0,751	0,749	0,75	0,751
	5	0,812	0,813	0,814	0,812	0,813	0,814
	6	0,873	0,874	0,875	0,873	0,874	0,875
	7	0,936	0,937	0,938	0,936	0,937	0,938

Table 5. Experimental results under different temperature conditions (Second part).

OAM	Test condition	V_{ref}[AV_{CC} units] 80ºC			V_{ref}[AV_{CC} units] 100ºC		
		Min	Mean	Max	Min	Mean	Max
	1	0,748	0,749	0,75	0,748	0,749	0,75
	2	0,499	0,5	0,501	0,499	0,5	0,5
	3	0,625	0,625	0,626	0,624	0,625	0,625
OA0	4	0,749	0,749	0,75	0,748	0,749	0,75
	5	0,812	0,813	0,813	0,811	0,812	0,813
	6	0,873	0,874	0,875	0,873	0,874	0,875
	7	0,936	0,937	0,938	0,936	0,937	0,938
	1	0,748	0,749	0,75	0,747	0,749	0,75
	2	0,499	0,5	0,501	0,499	0,499	0,50
	3	0,624	0,625	0,626	0,623	0,624	0,625
OA1	4	0,749	0,75	0,75	0,748	0,749	0,75
	5	0,812	0,813	0,813	0,811	0,812	0,813
	6	0,873	0,874	0,875	0,873	0,874	0,875
	7	0,936	0,937	0,938	0,936	0,937	0,938

The third evaluation tests the BIST strategy under different temperatures applied to the device. The test procedure is repeated 100 times for each test condition at 40ºC, 60ºC, 80ºC, and 100ºC. A temperature sensor embedded in the ADC module registers the temperature value. A detailed description of this sensor is provided by the manufacturer in [9]. Tables 4 and 5 report the maximum, minimum, and mean value

of the performed measurements. These tables show negligible differences and very low dispersion in the measurements for all the temperatures.

The last experiment evaluates the performance of the test strategy for different devices and determines chip-to-chip variations. For this experiment, the routine is evaluated in 10 devices MSP430F2274 under the same conditions of the first evaluation. Table 6 resumes the maximum and minimum values registered for each test condition, for all tested devices. The table shows the minimum and maximum value for the reference voltage and the error relative to the ideal evaluations presented in Table 2. As the previous evaluations, the measurements present very low dispersion for all the devices tested. In this case, the maximum inter-chip dispersion is ±0.4% for test condition 2 in OA1.

Table 6. Experimental results for different chips under test.

OAM	Test condition	Max V_{ref} [V_{CC} units]	Relative Error [%]	Min V_{ref} [V_{CC} units]	Relative Error[%]
OA0	1	0,751	0,133	0,748	-0,266
	2	0,501	0,2	0,499	-0,2
	3	0,626	0,16	0,623	-0,32
	4	0,751	0,133	0,748	-0,266
	5	0,814	0,184	0,81	-0,307
	6	0,876	0,114	0,873	-0,228
	7	0,938	0,053	0,935	-0,266
OA1	1	0,751	0,133	0,748	-0,266
	2	0,502	0,4	0,498	-0,4
	3	0,626	0,16	0,623	-0,32
	4	0,751	0,133	0,747	-0,4
	5	0,814	0,184	0,81	-0,307
	6	0,876	0,114	0,872	-0,342
	7	0,939	0,159	0,936	-0,159

5 Conclusions

This paper addressed a BIST strategy for a resistor array that belongs to an EACC of a modern μC. The main characteristic of the BIST is the use of only hardware and software resources of the μC that achieves a low cost test scheme. The test strategy is experimentally evaluated using commercial hardware provided by the vendor. Our experimental results show very good repeatability, with very low dispersion in one chip, a sample of ten chips and under different temperature conditions. The error of the measurements using a higher precision voltmeter is also low. These results allow concluding that the BIST proposed here is useful for testing the functionality of the resistor array in the EACC under test using a simple and very low cost strategy.

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