Analysis of a series resonant AC/DC converter with integral cycle mode control for high frequency AC distribution systems

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Abstract: **-** The study of a resonant AC/DC converter, thought for high frequency sinusoidal AC power distribution systems, is performed in this article. The control switch is commuted at the resonant current zero crossings, staying closed (or open) for a certain number of complete cycles. This commutation strategy, known as "integral cycle mode control", gives soft-switching which improves efficiency, minimizes EMI and increases reliability and converter life span. Also, the input current has a low THD and a good power factor.

A suitable scheme to control the converter is proposed. It consists of an internal loop based on sliding mode techniques, for regulating the amplitude of the resonant current, and an external PI loop with an added feed-forward action, that sets the DC output voltage. The main objective is minimizing the disturbing effect that variations in the AC bus voltage and load consumption have over the DC output voltage. For the design of the control laws, a model expressed in terms of rectified and averaged sinusoidal variables is employed.

Computer simulations have been performed, considering typical surrounding conditions for this kind of application. The obtained results show that the converter DC output voltage stay always close to its reference value, presenting good rejection against the aforementioned disturbances.

Key-Words: - High frequency AC distribution; AC/DC conversion; series resonant converter; integral cycle mode control; sliding mode control.

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1 Introduction

Currently, distribution of electrical energy in telecommunications systems, computer systems, electronic commercial systems and autonomous vehicles it is mostly performed using direct current (DC). Many researchers consider convenient the use of high frequency alternating current (HF AC) instead of DC for these applications [1] [2]. The most salient advantage of HF AC distribution systems over DC systems is the fewer number of conversion stages and transformers required. Therefore, they could have a higher efficiency, lower cost and greater reliability due to the lower parts number and less complexity. Likewise, it has been determined that systems that use a sinusoidal HF AC bus voltage are preferable, due to the lower EMI they produce.

A typical HF AC distribution system has two stages of conversion [3] [4]:

a) an inverter, that is responsible for generating the AC bus voltage from a battery (in the case of autonomous systems, for example a vehicle) or from the DC output of a rectifier (in the case of an on-line system, where the primary source of energy is the grid),
b) an AC/DC converter to supply each load with DC voltage.

In a previous work, the analysis and experimental evaluation of an AC/DC resonant converter, suitable for using at the load side of HF sinusoidal AC power distribution systems were presented [5]. In that article, a theoretical analysis of the converter operation in steady-state and continuous conduction mode (CCM) was performed. It was considered a fixed switch commutation angle, i.e., operation in open loop condition. Approximate mathematical expressions were deduced that allowed the prediction of the conversion ratio, the efficiency and the input current THD. A converter prototype was built and was included in a laboratory HF sinusoidal AC distribution system in order to validate the theoretical analysis and to investigate the performance under different working conditions.

In order to not contaminate the HF AC bus, it is desirable that the input current of the AC/DC converter has a low harmonic content, minimizing

conducted and radiated EMI. A good input power factor is also convenient, to minimize transmission losses [4].

One aspect that was thought that could probably be improved is the switch commutation strategy. In [5], the switch was commuted four times within the resonant cycle and at instants where the resonant current has somewhat high values. This results in hard-switching operation, which puts the converter in unfavorable conditions with respect to losses, EMI and reliability. On the other hand, appreciable variations in the DC output voltage were observed during the tests, when the load consumption or the HF AC distribution bus voltage changed. It was considered necessary to adopt a closed loop control system to keep the DC output voltage constant.

In the present article, the same converter topology of [5] is taken again but to overcome the problems encountered in the previous work, we are using now a different switching strategy, called "integral cycle mode control". In the past, other researchers have been applied this technique in DC/DC Quantum Resonant Converters (QRC) [6] [7]. Basically it consist in the commutation at the zero crossing of the resonant current, keeping the switch open (or closed) for a whole number of complete cycles. Accordingly, the semiconductor devices operate in soft switching, allowing the reduction of switching losses. As a consequence, a markedly improvement in the conversion efficiency could be expected. A minimization of EMI and an increased reliability and life span of the converter would have to be achieved. Also, in this switch commutation method the AC input current presents a good waveform quality, with low distortion and good power factor.

The present paper is organized in the following manner: the converter operation with integral cycle mode control is analyzed in Section 2. Considering the particular characteristics of this operation mode, a dynamic model for the converter expressed in terms of rectified and averaged sinusoidal variables is presented in Section 3. This type of model has been proposed by various authors and simplifies the process of designing the control loops [6] [7]. In Section 4 has been developed a closed loop control scheme for the converter, whose main objective is to regulate the DC output voltage, regardless of eventual voltage variations in the HF AC bus and variations of the current requested by the load. The good performance of this control scheme has been verified through simulations in various working conditions, the results of which are shown in Section 5. Finally, in Section 6, some conclusions of the work are drawn.

2 Converter operation

This section firstly presents a description of the AC/DC resonant converter circuit. Then, it is explained the principle of operation when the converter uses the "integral cycle mode control" mentioned above. Subsequently, a mathematical analysis is done, mainly focused on determining the amplitude of the resonant current for each state of the switch. At the section end, the condition that must be met to operate in CCM is established.

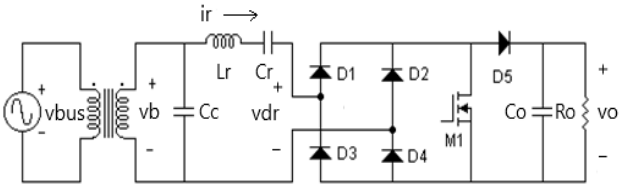

Fig.1. Circuit of the AC/DC series resonant converter.

2.1 Converter circuit description

The circuit of the converter under study is shown in Fig. 1. It has an input transformer to adapt voltage levels and a capacitor (C_c) in the secondary compensates the magnetization current to improve the input power factor (PF). A series resonant circuit (L_r-C_r), tuned to the AC bus frequency, makes the resonant current (i_r) to be sinusoidal and in phase with the AC bus voltage. Subsequently, i_r is rectified by means of a full-wave diode bridge (D1-D4), whose output is connected to a structure similar to that of the classical boost DC/DC converter. A switch (M1) derives the rectified i_r to ground when closed, controlling the portion of it that reaches the parallel circuit formed by the consumption load (R_o) and the capacitor (C_o). C_o maintains a low ripple in the DC output voltage (v_o), while a diode (D5) prevents C_o from being discharged when M1 is closed.

2.2 Converter operation principle

The analysis of the resonant converter presented here is carried out under certain simplifying hypotheses:

- The HF AC distribution bus is considered as an ideal voltage source that provides a purely sinusoidal voltage.
- The input transformer is considered ideal.
- The passive elements are mostly ideal; the only parasitic considered is R_r (total series resistance of L_r–C_r).
- The electronic devices are ideal: zero voltage drop in conduction and infinite resistance when open. The switching times are negligible

compared to the period of the HF AC bus voltage.
- The converter operates all the time in CCM, which means that i_r never extinguish.
- The output time constant (R_oC_o) is much greater than the maximum time in which M1 remains closed.

The most relevant voltage and current waveforms of the converter are shown in Fig. 2. The instantaneous voltage in the secondary of the transformer v_b, Fig. 2a, is:

$$v_b(t) = \hat{v}_b \sin(\omega_b t) \quad , \quad (1)$$

where:

$\hat{v}_b$: transformer secondary peak voltage,
$\omega_b=2\pi f_b$, f_b: AC bus frequency.

M1 is controlled by means of the command signal u that is synchronized with the zero crossings of the AC bus voltage, Fig. 2b (M1 is closed for u=1 and is open for u=0). M1 is kept closed for a certain number of complete cycles and maintained open for another number of complete cycles. This technique is known as "integral cycle mode control".

The L_r-C_r tank circuit is tuned to the AC bus frequency. This means that the resonant frequency (f_o) verifies (2) and, therefore, the impedance is zero at f_b.

$$f_o = \frac{1}{2\pi\sqrt{L_r C_r}} = f_b \quad (2)$$

The voltage at the input terminals of the diode bridge (v_{dr}) is zero when M1 is closed and is a square-wave whose amplitude is v_o, when M1 is open, Fig. 2c. This non-sinusoidal voltage waveform originates harmonics of f_b in the resonant current. As the tank circuit has high impedance a these frequencies, the harmonic componentes are of small amplitude.

Taking into account the tuning of the tank circuit given in (2), the frequency selectivity that presents its impedance, the fact that v_b is purelly sinusoidal (1) and that M1 is switched at zero crossings of v_b, all these reasons cause the resonant current to have an almost sinusoidal waveform that allways remains in phase with v_b:

$$i_r(t) = \hat{\imath}_r \sin(\omega_b t) \quad (3)$$

The amplitude of the resonant current ($\hat{\imath}_r$) increases when M1 is closed and decreases when M1 is open and that is why i_r presents an envelope similar to and AM signal, Fig. 2d.

The commutation of M1 at the zero crossings of v_b gives switching with zero current, because both are in phase.

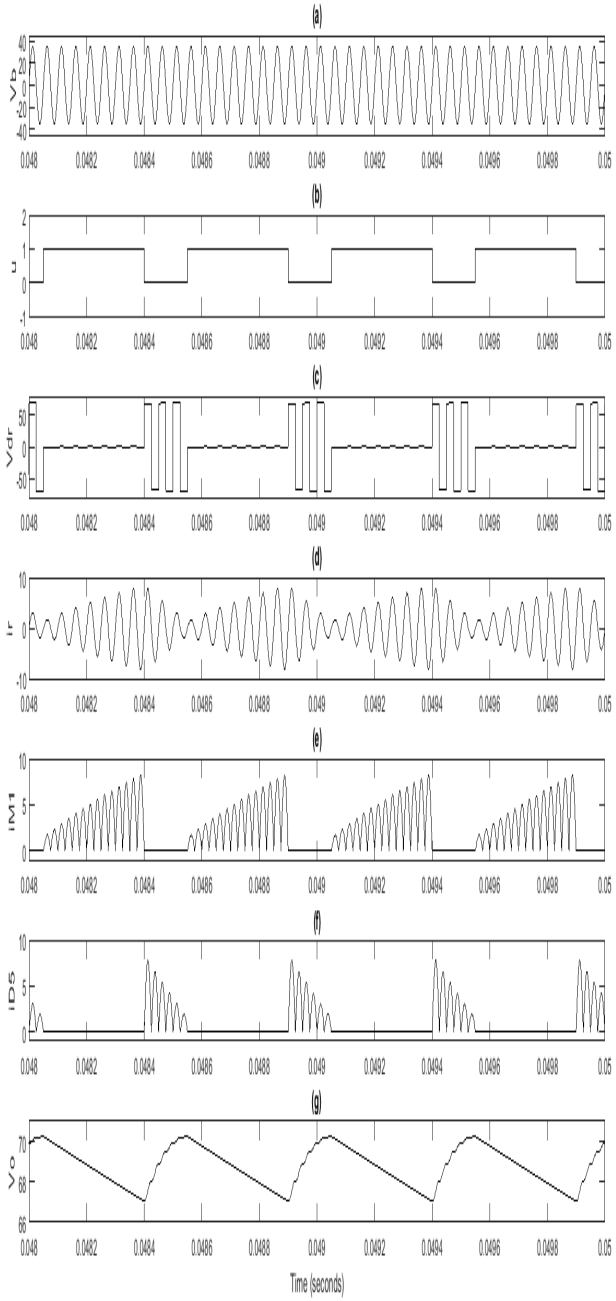

Fig. 2. Converter most relevant voltage and current waveforms. (a): transformer secondary voltage, (b): M1 control signal, (c): bridge rectifier input voltage, (d): resonant current, (e): M1 current, (f): D5 current, (g): DC output voltage.

In controlling the amplitude of the resonant current (which will be done in Section 4), it is important to know if a particular amplitude value can be attained. For this we must know the maximum and minimum amplitudes that the current can reach when the switch is kept permanently closed or open. This

limit values will be determined in the following paragraphs.

M1 closed

In this situation, i_r is derived to ground by M1, Fig. 2e, and v_{dr} is approximately zero, Fig. 2c, causing the amplitude of i_r to increase and as a result the stored energy in L_r-C_r becomes greater. If M1 remains closed for a sufficiently long time, the amplitude of i_r reaches a stationary condition and it has the highest possible value. As D1-D4 and M1 are considered ideal devices, the amplitude of i_r in steady-state is:

$$\hat{\imath}_{rss}|_{M1-on} = \hat{v}_b/R_r \qquad (4)$$

In (4) R_r is the total parasitic series resistance of L_r-C_r.

The mathematical expression of the instantaneous current during the turn-on transient of a series RLC circuit with a sinusoidal AC voltage source, is quite complex for a completely generic case. Fortunately, the situation of the AC/DC resonant converter under analysis it is very particular, as the tank circuit is tuned to the source frequency and the switch is turned-on at the source voltage zero crossing. Consequently, the general expression is greatly simplified and results:

$$i_r(t) = \{\hat{\imath}_{rss} - [\hat{\imath}_{rss} - \hat{\imath}_{ri}]e^{-\alpha t}\}sen(\omega t) \ , \qquad (5)$$

where:

$\hat{\imath}_{ri}$: initial amplitude of i_r.
α: $R_r/2L_r$, damping factor.

While M1 is closed, D5 is reversely biased and C_o keeps R_o powered, discharging slowly in approximately linear fashion (Fig. 2g). The voltage v_o will fall little if the C_o value is large enough, that is, if the output time constant (τ_o) satisfy the following inequality:

$$\tau_o = R_{omin}C_o \gg N_{max}/f_b \qquad , \qquad (6)$$

N_{max} being the maximum number of cycles in which M1 remains closed.

M1 open

When M1 is open, i_r is rectified by the diode bridge and then circulates trough D5 (Fig. 2f), supplying R_o and replenishing the charge of C_o, so v_o has a pseudo-sinusoidal ripple (Fig. 2g) in this interval. During this time, v_{dr} has a square waveform whose amplitude is v_o, in phase with i_r (Fig. 2c) due to the presence of the bridge rectifier D1-D4. The polarity of v_{dr} is opposite to that of v_b, decreasing the amplitude of i_r. The fundamental component of v_{dr} is:

$$v_{dr1}(t) = \hat{v}_{dr1}\ \text{sign}\{i_r(t)\} \qquad , \qquad (7)$$

where: $\hat{v}_{dr1} = 4\bar{v}_o/\pi$.

The harmonic content of v_{dr} causes the appearance of harmonic components in i_r, but they will be of relatively small amplitude due to the impedance that the tank circuit presents at these frequencies. To make an approximate calculation, these harmonic components can be ignored, using an approach known as "*sinusoidal analysis of resonant converters*" [8]. Considering also that the fundamental components of v_{dr} and i_r are in phase, it is possible to define an equivalent resistance (R_e) seen from the input terminals of the bridge rectifier bridge [8]:

$$R_e = \hat{v}_{dr1}/\hat{\imath}_r = \frac{8}{\pi^2}R_o \qquad (8)$$

Then, the steady-state amplitude ($\hat{\imath}_r$) of the resonant current when M1 is permanently open has the lower possible value and is:

$$\hat{\imath}_{rss}|_{M1-off} = \hat{v}_b/(R_r + R_e) \qquad (9)$$

As in steady-state the average current of C_o is zero, the average value of i_r (rectified) passes through R_o, determining the mean value of v_o:

$$\bar{v}_o = \bar{\imath}_r R_o = \frac{2}{\pi}\,\hat{\imath}_r R_o \qquad (10)$$

With M1 permanently open, the converter takes the minimum power level from the AC bus, since i_r has the lower amplitude. In this condition, the minimum $\bar{v}_o$ is developed, whose expression can be obtained by combining (8), (9) and (10):

$$\bar{v}_{omin} = \hat{v}_b/(\frac{4}{\pi} + \frac{\pi}{2}\frac{R_r}{R_o}) \qquad (11)$$

In normal operation and in steady-state, M1 is switched periodically and regularly since u will have a fixed pattern. In that situation, M1 will be closed and open for short periods of time and the limit values given by (4) and (9) will not be reached. The amplitude of the resonant current will have a triangular envelope (see Fig. 2e and Fig. 2f), and the amplitude average value will depends on the relationship between the time that u=1 with respect to the time that u=0. Accordingly, as this average amplitude will be between the limits (4) and (9), $\bar{v}_o$ will be greater than the value calculated in (11).

2.3 Condition for CCM operation

The worst situation for the converter to enter in the discontinuous conduction mode (DCM) is when M1 is permanently open. In this case, the converter behaves like the resonant rectifier studied in [9], and it operates in DCM if L_r is small or R_o large. The condition that the numerical values of these elements must meet to ensure operation in CCM can be found in [9]:

$$Q = \frac{Z_o}{R_o} \geq \frac{2}{\pi} \quad , \qquad (12)$$

where Q denotes the normalized quality factor and Z_o the characteristic impedance of the tank circuit, defined as:

$$Z_o = \sqrt{\frac{L_r}{C_r}} \qquad (13)$$

Equations (2), (12) and (13) allow sizing L_r and C_r to guarantee CCM even when the load consumption is at minimum (maximum R_o value). On the other hand, (6) allows sizing C_o by adopting an acceptable DC output voltage ripple. Its maximum value occurs when R_o is minimal.

3 Converter model

A standard dynamic model of the AC/DC series resonant converter, valid for both states of the switch, can be obtained applying Kirchoff laws to the circuit of Fig. 1:

$$\begin{cases} L_r \frac{di_r}{dt} + R_r i_r + \frac{1}{C_r}\int i_r dt = \hat{v}_b sen(\omega t) - (1-u) v_o sign(i_r) \\ C_o \frac{dv_o}{dt} + \frac{v_o}{R_o} = (1-u) abs(i_r) \end{cases} \qquad (14)$$

The model (14) is valid under the assumptions mentioned in Section 2.2. It is formed by two differential equations of the state variables i_r and v_o. From considering the peculiar characteristics of the resonant converter under study, the model (14) can be simplified. Foremost, taking into account the analysis done in Section 2, let's assume that that i_r is a sinusoid with variable amplitude over time (3). It is also known that in a sinusoidal waveform the half-cycle average value is related to the amplitude by a numerical constant ($2/\pi$). It is therefore advantageous to employ a dynamical model that describes only the temporal evolution of the half-cycle average value of i_r rectified [6] [7]. At this point, it is opportune to remember that the amplitude of i_r depends on the AC bus voltage (1) and the fundamental component of v_{dr} (7), both sinusoidal quantities that can be rectified and averaged too, in a half-cycle basis.

Regarding v_o, it is also possible to model the variation of its average value only, based on the "small ripple hypothesis" [8]; situation that usually occurs if C_o is correctly sized.

Therefore, we will take the half-cycle averaged quantities $\bar{\imath}_r$ and $\bar{v}_o$ as the new state variables. These variables are easily determined, measuring their instantaneous electrical values and performing a simple numerical averaging in half-cycle time period basis (for i_r, their absolute value must first calculated). Then, the simplified dynamic model becomes:

$$\begin{cases} \frac{d\bar{\imath}_r}{dt} = -\frac{16\bar{v}_o}{\pi^2 L_r} + \frac{2\bar{v}_b}{L_r} - \frac{2R_r\bar{\imath}_r}{L_r} + \frac{16\bar{v}_o}{\pi^2 L_r}.u \\ \frac{d\bar{v}_o}{dt} = \frac{\bar{\imath}_r}{C_o} - \frac{\bar{v}_o}{R_o C_o} - \frac{\bar{\imath}_r}{C_o}.u \end{cases} , \qquad (15)$$

where:

$$\bar{\imath}_r = \frac{2\hat{\imath}_r}{\pi} \ , \ \bar{v}_b = \frac{2\hat{v}_b}{\pi} \ , \ \bar{v}_{dr1} = \frac{2\hat{v}_{dr1}}{\pi} = \frac{8\bar{v}_o}{\pi^2} \qquad (16)$$

Making u=1 it is easy to see that (15) is consistent with the time response of i_r given by (4) in Section 2.

Looking at (15), it is evident that we are in the presence of a non-linear system, of the form:

$$\dot{x} = f(x) + g(x).u \quad , \qquad (17)$$

where:

$$f(x) = \begin{bmatrix} -\frac{16\bar{v}_o}{\pi^2 L_r} + \frac{2\bar{v}_b}{L_r} - \frac{2R_r\bar{\imath}_r}{L_r} \\ \frac{\bar{\imath}_r}{C_o} - \frac{\bar{v}_o}{R_o C_o} \end{bmatrix} \quad g(x) = \begin{bmatrix} \frac{16\bar{v}_o}{\partial^2 L_r} \\ -\frac{\bar{\imath}_r}{C_o} \end{bmatrix}$$

4 Control strategy

A simple analysis demonstrates that v_o is a non-minimum phase variable. Indeed, for an increase of the time in which M1 remains closed, what occurs first is the fall of v_o, since the discharge time of C_o is instantly augmented. Then, when the amplitude of i_r increases, v_o start to rise. Therefore, to control v_o is necessary to do it indirectly through another variable.

For this reason, it was decided to employ an internal control loop that sets the half-cycle average value of i_r, following a reference that comes from an external loop that regulates $\bar{v}_o$. To implement this internal current loop, the sliding mode control (SMC) technique was chosen due to its good properties with respect to rejection of disturbances and its

robustness against parameters changes [10]. The selected sliding surface *S(x)* is:

$$S(x) = \bar{\imath}_{ref} - \bar{\imath}_r \quad , \quad (18)$$

and the command signal of M1 is the discontinuous control action *u*:

$$u = \begin{cases} 1 & if \ S(x) > 0 \\ 0 & if \ S(x) < 0 \end{cases} \quad (19)$$

To make the SMC of $\bar{\imath}_r$ possible, the transversality condition $L_gS<0$ must be verified:

$$L_g\mathrm{S} = \ \mathrm{S.g} = -16\bar{v}_o/\eth^2 L_r < 0 \quad , \quad (20)$$

where L_gS is the derivative of Lie in the g direction. In this case it is verified, since $\bar{v}_o>0$.
The equivalent control is given by:

$$u_{eq} = -L_f\mathrm{S}/L_g\mathrm{S}=1-\frac{\bar{v}_b - R_r\bar{\imath}_r}{\frac{8}{\eth^2}\bar{v}_o} \quad (21)$$

In order to work in SM, the necessary and sufficient condition is that u-<u_{eq}<u+, that is:

$$0<1-\pi^2(\bar{v}_b - \mathrm{R_r}\bar{\imath}_r)/8\bar{v}_o <1 \quad (22)$$

Equation (22) can be rearranged as:

$$\frac{\hat{v}_b}{\mathrm{R_r}+\frac{8}{\pi^2}R_0} < \bar{\imath}_r < \frac{\hat{v}_b}{\mathrm{R_r}} \quad , \quad (23)$$

indicating that $\bar{\imath}_r$ can be controlled by SM if the desired value is within the limits imposed by (4) and (9).
It remains to verify the stability of $\bar{v}_o$ when $\bar{\imath}_r$ is in SM. To do this we replace u_{eq} given by (21) in (15), taking into account that in this condition $\bar{\imath}_r = \bar{\imath}_{ref}$, obtaining:

$$\begin{cases} \frac{d\bar{\imath}_r}{dt} = 0 \\ \frac{d\bar{v}_o}{dt} = -\frac{\bar{v}_o}{R_oC_o} + \frac{\bar{\imath}_{ref}}{C_o}\left(\frac{\bar{v}_b - R_r\bar{\imath}_{ref}}{\bar{v}_o}\right)\frac{\eth^2}{8} \end{cases} \quad (24)$$

The equilibrium point of $\bar{v}_o$ is obtained forcing $\frac{d\bar{v}_o}{dt}$=0. Applying this condition to (24), and expressing sinusoidal quantities in terms of its peak values, it results:

$$\bar{v}_{oss}{}^2/R_o = \hat{v}_b\hat{\imath}_{ref}/2 - R_r\hat{\imath}_{ref}{}^2/2 \quad (25)$$

Equation (25) means that when $\bar{v}_o$ reaches its stationary value, the load power is equal to the power delivered by the AC bus discounting the loss in R_r. It only remains to check if the $\bar{v}_{oss}$ of (25) is stable. Graphing $\frac{d\bar{v}_o}{dt}$, given in (24), as a function of $\bar{v}_o$, it is easy to verify that $\bar{v}_{oss}$ is stable, since it satisfies:

$$\frac{d\bar{v}_o}{dt}: \begin{cases} > 0 & if \quad \bar{v}_o < \bar{v}_{oss} \\ = 0 & if \quad \bar{v}_o = \bar{v}_{oss} \\ < 0 & if \quad \bar{v}_o > \bar{v}_{oss} \end{cases} \quad (26)$$

In the implementation of the SM controller, a sample and hold circuit is used, which is triggered at each zero crossing of the AC bus voltage. This keeps the value of *u* (19) constant within each period of v_b, preventing the deformation of the resonant current waveform. As a disadvantage, the sample and hold circuit introduces a time delay that causes the appearance of "chattering" in $\bar{\imath}_r$, which can be seen in the simulations results presented in Section 5.
A slow external loop, based on a PI controller with anti-windup, generates an intermediate reference $\bar{\imath}_{PI}$:

$$\bar{\imath}_{PI} = K_P\left(\bar{v}_{oref} - \bar{v}_o\right) + K_I\int\left(\bar{v}_{oref} - \bar{v}_o\right) \quad (27)$$

In order to improve the rejection of AC bus voltage variations, this intermediate reference $\bar{\imath}_{PI}$ is modulated by a multiplicative type feed-forward controller. In this manner, the reference for the SMC current loop is:

$$\bar{\imath}_{ref} = (\bar{v}_b/\bar{v}_{b\_rated})\bar{\imath}_{PI} \quad , \quad (28)$$

being $\bar{v}_{b\_rated}$ the half cycle averaged value of the rated AC bus voltage.

Finally, the reference for the SMC current loop (28) is limited by saturation, between a value greater than the minimum possible at steady-state given by (9) to ensure controllability and a value below the maximum possible given by (4), to protect the components of the converter avoiding exceeding their maximum ratings.

5 Simulation results

Simulations were carried out with the intention of verifying the correct operation of the "integral cycle mode control" and the suitability of the proposed control scheme to regulate $\bar{v}_o$. Better results could be obtained, using an AC bus with higher frequency,

optimizing the design of the converter components and with a finer adjustment of the controllers.
The converter was modeled using functional elements available in the SimPowerSystems library of the graphical programming environment Simulink/MATLAB®. The values of the parameters used are shown in Table1. With the exception of C_o, the rest of the values are the same as those used in [5].

v_b	25Vrms +/- 20%
f_b	20KHz
L_r	649.9µH
C_r	97.4nF
R_r	1.76Ω
C_o	200µF
R_o	25Ω - 50Ω

Table 1. Converter parameters.

A first simulation was conducted using the converter in open-loop. Although it was not said before, the results are those that have already been shown in Fig. 2. A fixed pattern for the control signal u was adopted, keeping M1 closed for seven complete cycles (t_{on}=350us) and open for three complete cycles (t_{off}=150us), see Fig. 2b. This signal has been synchronized with the zero crossings of the transformer secondary voltage showed in Fig. 2a.
The correct commutation of M1 can be observed in Fig. 2e and that the resonant current is not extinguished (CCM), in Fig. 2d. With a load resistance of R_o=40Ω the resulting average DC output voltage is $\bar{v}_o$=68.5V, that is quite greater than $\bar{v}_{omin}$=26.4V, value obtained using (11). The ripple in the DC output voltage is 3V peak to peak, Fig. 2g.
Once it was known that the converter operates in open loop as expected, the control scheme proposed in Section 4 was added. In a first step only the SMC current loop was applied and the results are shown in Fig. 3.The averaged current reference was a step from 2A to 5A at t=0.1s, Fig. 3b. The introduced disturbances were an abrupt decrease of the load, from 50Ω to 25Ω at t=0.05s, and a sudden increase in v_b, of + 20% at t=0.15s, represented in Fig. 3a. In Fig. 3c it is shown the average value of the rectified resonant current and that can be appreciated how it practically does not change in spite of the detrimental effects of these disturbances, and follows closely the reference of Fig. 3b. Notwithstanding, a significant "chattering" is clearly visible. As mentioned above, this is due to the relatively low frequency of the AC bus used in simulations. The variation of v_o, that can be observed in Fig. 3d, it is completely expected since it is not controlled. For a current reference of 2A and with a 50Ω load, an average DC output voltage of about 48V is obtained. Paying special attention at t=0.1s the non-minimum phase behavior of v_o can be noticed.
In a second step, a simulation was performed adding the output voltage controller to the SMC current controller, as was discussed in Section 4. For the voltage controller tuning, conventional techniques were used. The resulting gain values were K_P=0.1 and K_I=100 and the DC output voltage reference was set at 48V. Fig.4 depicts how an abrupt decrease in the AC bus voltage, of -20% starting at t=0.05s (Fig. 4a), affects the regulated DC output voltage (Fig. 4b). A momentary voltage drop of the order of 1V is observed and then the reference value is reached again in approximately 5ms.

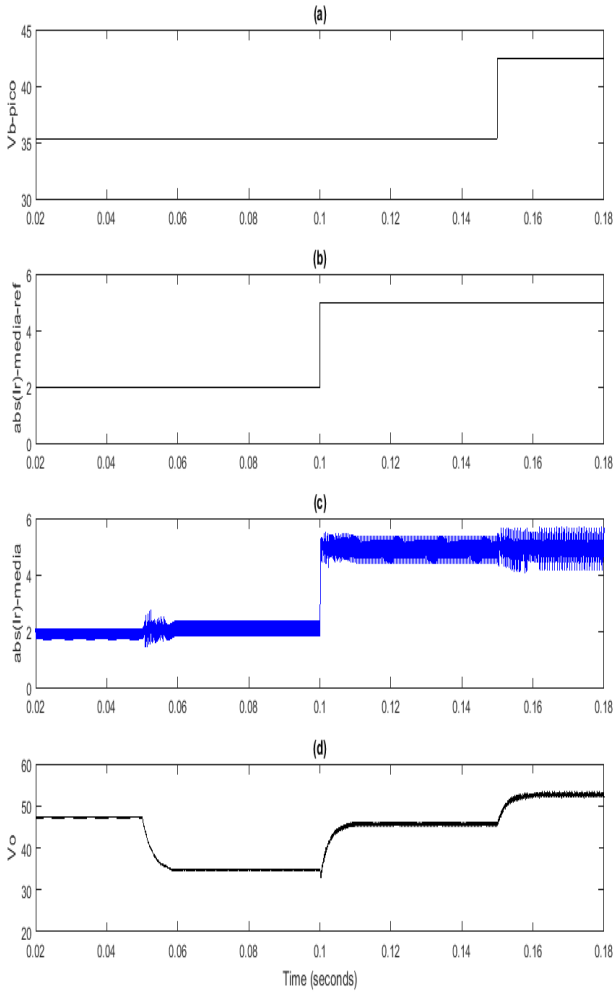

Fig. 3. Response of the inner SMC current loop. (a): transformer secondary voltage amplitude, (b): reference for the SMC current loop, (c): resonant current, rectified and averaged, (d): DC output voltage.

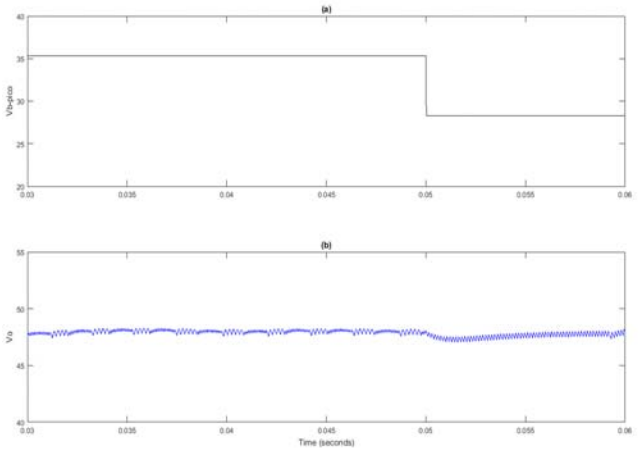

Fig. 4. Output voltage variation facing an abrupt AC bus voltage change. (a): transformer secondary voltage amplitude, (b): converter DC output voltage.

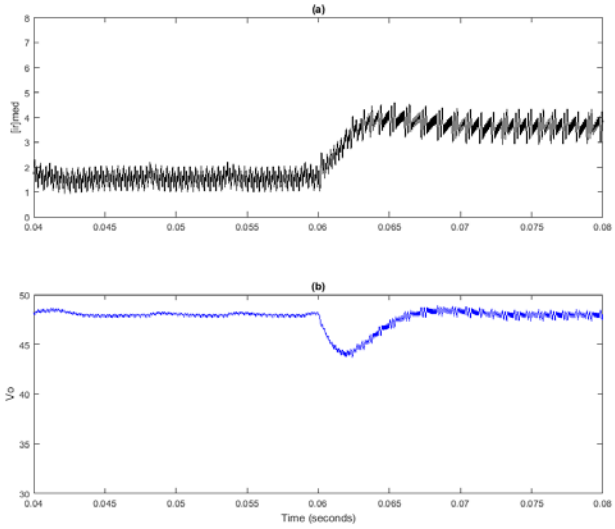

Fig. 5. Output voltage variation facing an abrupt load change. (a): resonant current, rectified and averaged, (b): converter DC output voltage.

6 Conclusions

In this article, the study of an LC series resonant AC/DC converter, using "integral cycle mode control", has been presented. A control scheme for the regulation of the converter DC output voltage was proposed. For the design of the control laws, a model expressed in terms of rectified and averaged sinusoidal variables was employed.

Compared to the previous work [5], based on the same converter but with another switching strategy, the mayor improvements that can be mentioned are: a) the circuit for the control and synchronization of the switch is much easier to implement, b) lower EMI and higher efficiency, due to the soft-commutation and c) the input current still having low THD and good power factor.

In principle, the "integral cycle mode control" has two small drawbacks: a) the resonant current exhibit amplitude changes (chattering) requiring some oversizing of the components to withstand the maximum amplitude condition; b) a somewhat larger than usual capacitor filter is required in order to obtain an acceptable output voltage ripple. This is because the switch could be closed during several cycles in some operating conditions. Nonetheless, both disadvantages can be minimized increasing the AC bus frequency.

Even based on a not optimized design example, the simulations performed shown an acceptable recovery time of the controlled DC output voltage facing two typical disturbances: AC bus voltage variations and load changes. This proves that the proposed control system operates satisfactorily.

It is worth to mention an additional advantage presented by the proposed control scheme: a highly reliable operation. As the current is limited, dangerous values that may fall outside the safe operating area of the various components of the converter are prevented.

It is appropriate to emphasize that the work has demonstrates the convenience of employing a dynamic model expressed in terms of rectified and averaged sinusoidal variables, to deduce the control laws for this kind of converters.

Finally, as a general comment, the authors believe that the converter, operated and controlled as proposed, has very good characteristics for the use at the load-end of power distribution systems based on a high frequency sinusoidal AC voltage bus.

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