A Fully-Differential DC Restoration Circuit

Enrique Spinelli and Alejandro Veiga
LEICI, Depto de Electrotecnia, Facultad de Ingeniería, Universidad Nacional de La Plata and
Consejo Nacional de Investigaciones Científicas y Técnicas (CONICET), La Plata, Argentina.
spinelli@ing.unlp.edu.ar

***Abstract*—Modern instrumentation is moving towards fully differential conditioning circuits. They provide an elegant and efficient way to adapt differential signals, like those provided by balanced sensors, to differential-input analog-to-digital converters (ADC). For that to be possible, many well-known Single-Ended (SE) conditioning circuits must be converted to their Fully-Differential (FD) versions. This work presents a FD dc servo circuit, able to restore both common mode and differential mode dc levels to their desirable values, suited to those required by the ADC to optimize its input range. The general scheme and the design procedure to adapt the circuit to particular needs are presented. Also experimental data obtained from a FD dc restoration circuit are presented.**

Keywords— fully-differential circuit; dc restoration; dc servo amplifier; common mode rejection ratio.

I. INTRODUCTION

DC restoration is a usual analog processing task, often used to reject signal dc components and amplifier offset voltages, ensuring a dc baseline level that allows fully exploiting the input range of analog stages or ADCs. This technique rejects unknown and variable dc components to establish a proper dc level. A general scheme of this kind of circuit is shown in Fig. 1 (a). The circuit output V_o is compared with the desired dc value (V_{REF}), the difference is integrated and feedback to the input. By this way, the dc output level equals to V_{REF} and the resulting transfer function is:

$$T(s) = \frac{\tau_i}{1 + s \cdot \tau_i / G} \tag{1}$$

The more usual circuit is based on an inverter amplifier topology [1], it presents low input impedance and is not appropriate for front-ends, which generally require high input impedances. A single-ended (SE) dc restoration topology based on the non-inverter topology (high input impedance) is presented in Fig.1 (b) [2].

Single-ended conditioning circuits are suited for unbalanced sensors, but not for balanced ones, like bridge sensors, that provide differential outputs. A common solution is to convert the differential signal to SE using a differential amplifier, and then process by SE circuits (i.e. restoring dc levels). Furthermore, current high resolution ADCs have differential inputs, requiring to reconvert the processed SE signals to differential mode again, before being connected to the ADC. These multiple conversions inevitably lead to signal degradation and also to a reduction of the dynamic range [3].

A natural and well-suited alternative is to use FD circuits for conditioning differential output sensors to differential input ADCs [4]. Moreover, FD circuits have higher dynamic range than their SE counterparts; they are ideally insensitive to variations on ground potential along the printed circuit board traces, and are well-suited to manage bipolar voltages by single voltage power-supplies (among other advantages). These are some of the reasons why instrumentation circuits trend is moving toward fully-differential topologies.

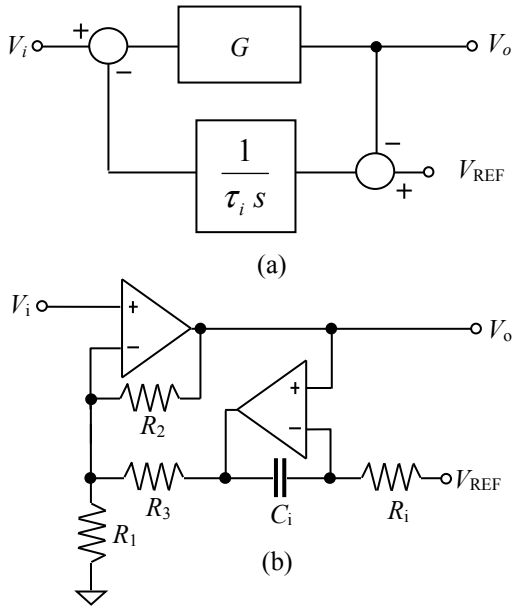

Fig. 1. (a) General scheme of a dc restoration circuit and (b) a Single-Ended circuit that implements it.

Fully-Differential circuits work with both Differential Mode (DM) and Common Mode (CM) voltages. When DM (v_{iD}) and CM (v_{iC}) voltages are applied to the input, DM (v_{oD}) and CM (v_{oD}) voltages appear at the output. Differential v_D and common mode voltages v_C are defined in terms of ground-referenced voltages v_H, v_L at the circuit's nodes by:

$$v_D = v_H - v_L \;;\; v_C = 0.5\left(v_H + v_L\right) \tag{2}$$

The input-output voltage relationship can be expressed as:

$$v_{oD} = G_{DD} v_{iD} + G_{DC} v_{iC}$$
$$v_{oC} = G_{CD} v_{iD} + G_{CC} v_{iC} \quad (3)$$

where G_{DD} represents the DM gain and G_{CC} the CM gain [5]. Expression (3) can be presented in a more compact form denoting differential and common mode voltages as components of a voltage vector (in capital letters):

$$V_o = G \cdot V_i \quad (4)$$

The cross-terms G_{DC} and G_{CD}, related to mode's transformations, are ideally zero, but in practice they have non-null values due to component unbalances. The main merit factor for FD circuits is the well-known Common Mode Rejection Ratio (CMRR) defined as:

$$CMRR = \frac{G_{DD}}{G_{DC}} \quad (5)$$

Avoiding grounded elements it is possible to design FD circuits for ultra high CMRR [6], but this approach leads to a unity G_{CC} and is not feasible to conditioning CM voltages, which are ground-referred potentials. This work presents a FD circuit that implements the scheme of Fig. 1(a). It processes DM and CM voltages, thus allowing to restore dc levels for both modes.

II. PROPOSED CIRCUIT

The proposed circuit, presented in Fig. 2, is a fully-differential version of that in Fig. 1(b), which was adopted as starting SE prototype. This FD topology was obtained by mirroring and coupling the SE prototype according to [6].

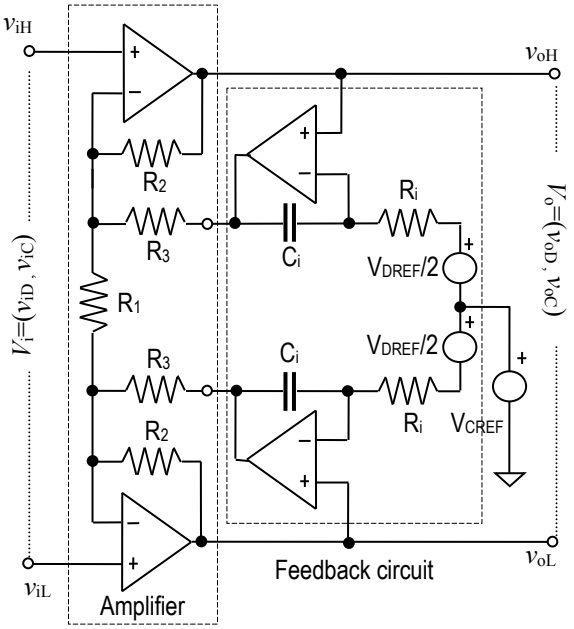

Fig. 2. Proposed circuit for dual mode dc restoring. It sets at its output V_{DREF} and V_{CREF} dc levels for DM and CM respectively.

The circuit can be decomposed in a FD difference amplifier G and a FD feedback network H connected as indicated in the circuit of Fig. 2. Figure 3 shows the same idea but in an schematic form.

The amplifier G has two inputs V_i , V_{FB} and one output V_o. Its input-output relationship can be expressed as:

$$V_o = \begin{bmatrix} G_1 & G_2 \end{bmatrix} \cdot \begin{bmatrix} V_i \\ V_{FB} \end{bmatrix}, \quad (6)$$

where the matrix gain elements are given by:

$$G_{DD1} \cong 1 + \frac{2 \cdot \overline{R}_2}{R_1 // 2\overline{R}_3} \; ; \; G_{DC1} = \frac{R_2}{R_3} - \frac{R'_2}{R'_3}$$
$$G_{CC1} \cong 1 + \frac{\overline{R}_2}{\overline{R}_3} \; ; \; G_{CD1} = \frac{1}{2} \cdot \left(\frac{R_2}{2R_3} - \frac{R'_2}{2R'_3} + \frac{R_2 - R'_2}{R_1} \right) \quad (7)$$
$$G_{DD2} \cong -\frac{\overline{R}_2}{\overline{R}_3} \; ; \; G_{DC2} = -\left(\frac{R_2}{R_3} - \frac{R'_2}{R'_3} \right)$$
$$G_{CC2} \cong -\frac{\overline{R}_2}{\overline{R}_3} \; ; \; G_{CD2} = \frac{1}{2} \cdot \left(\frac{R_2}{2R_3} - \frac{R'_2}{2R'_3} \right)$$

and $\overline{R}_i$ denotes the average value of component R_i.

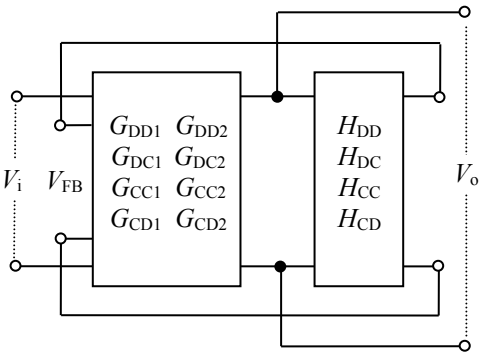

Fig. 3. Proposed circuit as interconnected matrix gain building blocks.

The feedback circuit (see Fig. 2) presents a pole at the origin and provides the AC coupling feature to the composed amplifier. This circuit is FD and the elements of its matrix gain H are given by:

$$H_{DD} \cong 1 + \frac{1}{s\overline{R}_i\overline{C}_i} \; ; \; H_{DC} = \frac{1}{s}\left(\frac{1}{R_i C_i} - \frac{1}{R'_i C'_i} \right)$$
$$H_{CC} \cong 1 + \frac{1}{s\overline{R}_i\overline{C}_i} \; ; \; H_{CD} = \frac{1}{4s}\left(\frac{1}{R_i C_i} - \frac{1}{R'_i C'_i} \right) \quad (8)$$

A. Differential Mode Gain

Solving the scheme of Fig.3 for differential mode voltages results in:

$$v_{oD} = v_{iD} G_{DD1} + v_{FBD} G_{DD2}$$
$$v_{FBD} = v_{oD} H_{DD} \quad (9)$$

and the DM gain A_{DD}:

$$A_{DD} = \frac{v_{oD}}{v_{iD}} = \frac{G_{DD1}}{1 - G_{DD2} H_{DD}} \quad (10)$$

Replacing the expressions of G_{DD1}, G_{DD2} and H_{DD} (7), (8):

$$A_{\mathrm{DD}} = \frac{A_{DD0}\tau \mathrm{s}}{1+\mathrm{s}\tau} \tag{11}$$

where:

$$A_{\mathrm{DD0}} = 1 + 2\frac{R_2 // R_3}{R_1}\ ;\ \tau = \left(1 + R_3/R_2\right) R_{\mathrm{i}} C_{\mathrm{i}} \tag{12}$$

B. Common Mode Gain

By a similar procedure, the CM mode gain A_{CC} results:

$$A_{\mathrm{CC}} = \frac{v_{\mathrm{oC}}}{v_{\mathrm{iC}}} = \frac{G_{\mathrm{CC1}}}{1 - G_{\mathrm{CC2}} H_{\mathrm{CC}}}, \tag{13}$$

$$A_{\mathrm{CC}} = \frac{\tau \mathrm{s}}{1+\tau \mathrm{s}} \tag{14}$$

C. Common Mode Rejection Ratio.

In order to find the overall *CMRR*, as a first step the CM-to-DM Gain A_{DC} must be calculated. If a common mode voltage v_{iC} is applied to the amplifier input, neglecting second order effects as double conversion factors, the differential and common mode output voltages (v_{oD}, v_{oC}), are:

$$\begin{aligned} v_{\mathrm{oD}} = v_{\mathrm{iC}} G_{\mathrm{DC1}} + v_{\mathrm{oD}} H_{\mathrm{DD}} G_{\mathrm{DD2}} + \\ + v_{\mathrm{oC}} \left(H_{\mathrm{CC}} G_{\mathrm{DC2}} + H_{\mathrm{DC}} G_{\mathrm{DD2}} \right) \end{aligned} \tag{15}$$

$$v_{\mathrm{oC}} = v_{\mathrm{iC}} G_{\mathrm{CC1}} + v_{\mathrm{oC}} G_{\mathrm{CC3}} G_{CC2} \tag{16}$$

Solving v_{oC} from (16), replacing it in (15), and using that $G_{\mathrm{CC2}}=G_{\mathrm{DD2}}$, $H_{\mathrm{CC}}=H_{\mathrm{DD}}$, $G_{\mathrm{DC2}}=-G_{\mathrm{DC1}}$ and $G_{\mathrm{DD2}}+G_{\mathrm{CC1}}=1$, the gain A_{DC} results:

$$A_{\mathrm{DC}} = \frac{\left(1 - H_{\mathrm{DD}}\right)}{\left(1 - H_{\mathrm{DD}} G_{\mathrm{DD2}}\right)^2} G_{\mathrm{DC1}} + \frac{G_{\mathrm{CC1}} G_{\mathrm{DD2}}}{\left(1 - H_{\mathrm{DD}} G_{\mathrm{DD2}}\right)^2} H_{\mathrm{DC}} \tag{17}$$

Replacing (7) and (8) in (17):

$$A_{\mathrm{DC}} = \frac{v_{\mathrm{oD}}}{v_{\mathrm{oC}}} = A_{\mathrm{DC0}} \cdot \frac{\mathrm{s}}{\left(1+\mathrm{s}\tau\right)^2}, \tag{18}$$

with

$$A_{\mathrm{DC0}} = -\left[\left(1 - \frac{R_2' R_3}{R_2 R_3'}\right) + \left(1 + \frac{\bar{R}_2}{\bar{R}_3}\right)\left(1 - \frac{R_i C_i}{R_i' C_i'}\right)\right] \frac{\bar{R}_3 \bar{R}_i \bar{C}_i}{\bar{R}_2}$$

Assuming resistors and capacitors with tolerances t_{R} and t_{C} respectively, the maximum value of A_{DC0} (worst case) is given by:

$$A_{\mathrm{DC0}} \le 2\tau \left(t_{\mathrm{R}} \left(\bar{R}_2 + 3\bar{R}_3\right) \Big/ \left(\bar{R}_2 + \bar{R}_3\right) + t_{\mathrm{C}}\right) \tag{19}$$

Expression (18) only considers passive component unbalances. Adding the effects of finite CMRR operational amplifiers (OA), it becomes:

$$A_{DC} = A_{\mathrm{DC0}} \frac{\mathrm{s}}{\left(1+\mathrm{s}\tau\right)^2} + \left(\frac{1}{CMRR_{\mathrm{A1}}} - \frac{1}{CMRR_{\mathrm{A2}}}\right) A_{\mathrm{DD}} \tag{20}$$

where $CMRR_{\mathrm{Ai}}$ denotes the common mode rejection ratio of the OA composing the front-end amplifier *G*. Finally, from (11) and (18) it is possible to find the overall *CMRR*:

$$CMRR^{-1} = \frac{A_{\mathrm{DC0}}}{A_{\mathrm{DD0}}} \frac{1/\tau}{\left(1+\mathrm{s}\tau\right)} + \left(\frac{1}{CMRR_{\mathrm{A1}}} - \frac{1}{CMRR_{\mathrm{A2}}}\right), \tag{21}$$

D. Differential DC input Range

An important feature of a dc restoring system is its dc input range. This means the maximum dc level at the input that the circuit could manage and reject. The differential output voltage v_{oD} of the input amplifier *G* can be expressed as a function of the DM voltage of its two inputs v_{iD}, v_{FBD} as:

$$v_{\mathrm{oD}} = v_{\mathrm{iD}} G_{\mathrm{DD1}} + v_{\mathrm{FBD}} G_{\mathrm{DD2}} \tag{22}$$

In the limit of the range of operation, v_{FBD} takes the maximum possible differential voltage $v_{\mathrm{FBD}}=\pm(V_{CC}-V_{DD})$, while $v_{\mathrm{iD}}=v_{\mathrm{iDDC}}$. Then, as the dc suppression system is working, it corrects the output voltage to $v_{\mathrm{oD}}=0$. In this situation, (22) becomes:

$$0 = v_{\mathrm{iDDC}} G_{\mathrm{DD1}} \pm \left(V_{CC} - V_{DD}\right) G_{\mathrm{DD2}}, \tag{23}$$

and the maximum admissible $v_{i\mathrm{DDC}}$ results in:

$$v_{\mathrm{iDDC}} = \pm\left(V_{\mathrm{CC}} - V_{\mathrm{DD}}\right) \frac{G_{\mathrm{DD2}}}{G_{\mathrm{DD1}}}. \tag{24}$$

Using (7) and (12), it is possible to express v_{iDDC} as a function of the nominal differential gain A_{DD0} and the R_3/R_2 ratio as:

$$v_{\mathrm{iDDC}} = \frac{\pm\left(V_{CC} - V_{DD}\right)}{A_{\mathrm{DD0}}\left(1 + R_3/R_2\right)} \tag{25}$$

E. Design example

As a design example, an amplifier with gain A_{DD0}=100, dc input range of ±120mV, V_{CC}=12V, V_{DD}=-12V and cutoff frequency lower than 0.1 Hz, will be described. Given the dc input range v_{iDDC} and the nominal gain A_{DD0}, the ratio R_3/R_2 can be found from (25) as:

$$R_3/R_2 = \frac{\left(V_{\mathrm{CC}} - V_{\mathrm{DD}}\right)}{v_{\mathrm{iDDC}} \cdot A_{\mathrm{DD}}} - 1 \cong 1 \tag{26}$$

Then, the ratio R_2/R_1 can be obtained from (12):

$$R_2/R_1 = 0.5\left(1 + R_2/R_3\right)\left(A_{\mathrm{DD}} - 1\right) \cong 100 \tag{27}$$

These resistor relationships can be fulfilled, for example, with R_2=220kΩ, R_3=220kΩ, R_1=2200Ω. Finally, to achieve the cutoff frequency of 0.1 Hz (τ=1.6 s), according to (12):

$$R_{\mathrm{i}} C_{\mathrm{i}} \left(1 + R_3/R_2\right) = 1.6\mathrm{s}, \tag{28}$$

that for R_3/R_2=1 results in:

$$R_{\mathrm{i}} C_{\mathrm{i}} = 0.8\ \ s. \tag{29}$$

In order to provide a margin for component tolerances, the values R_{i}=820 kΩ, C_{i}=1 μF were adopted, resulting a nominal cutoff frequency slightly lower than 0.1 Hz. Finally, the

component values are: R_1=2.2 kΩ, R_2=220 kΩ, R_3=220 kΩ, R_i=820 kΩ, C_i=1 µF.

F. Experimental validation

The circuit was built using 2% tolerance resistors, 10% tolerance capacitors, and general-purpose LF353 OAs. No selection was made and the component values were:

$$\begin{aligned} &C_i = 1.15\mu\text{F},\ C_i' = 1.12\mu\text{F},\ R_i = 816.5\text{k}\Omega, \\ &R_i' = 809.4\text{k}\Omega,\ R_2 = 218.0\text{k}\Omega,\ R_2 = 215.4\text{k}\Omega, \\ &R_3 = 214.2\text{k}\Omega,\ R_3' = 215.3\text{k}\Omega,\ R_1 = 2202\Omega. \end{aligned} \quad (30)$$

According to (11), (14) y (21), the main amplifier transfer functions A_{DD}, A_{CC} and its *CMRR* are:

$$A_{DD} = \frac{v_{oD}}{v_{iD}} = \frac{182.1\text{s}}{1+\text{s}1.84};\ A_{CC} = \frac{1.84\text{s}}{1+\text{s}1.84}, \quad (31)$$

$$CMRR^{-1} = 3862\left(1+\text{s}\tau\right)+\left(\frac{1}{CMRR_{A1}}-\frac{1}{CMRR_{A2}}\right) \quad (32)$$

In Fig. 7, the differential A_{DD} gain given by (31) and the measured data are shown. Finally, Fig. 8 shows the experimentally obtained *CMRR*. Both experimental results show a good agreement with those predicted by expressions (31) and (32).

III. Conclusions

An FD circuit that restores dc level for both differential mode and common mode voltages was proposed. It allows setting proper dc voltages to fully exploit the input range of current differential input ADCs. Its *CMRR* is moderate at low frequencies (around 70 dB), but increases up to 110 dB for higher frequencies, where it is limited by operational amplifiers *CMRR* unbalances.

There is a trade-off between *CMRR* and dc input range. Reducing resistor R_1 value increases differential mode gain A_{DD} and *CMRR*, but reduces the maximum dc input range. Analytic design equations were provided and experimentally validated.

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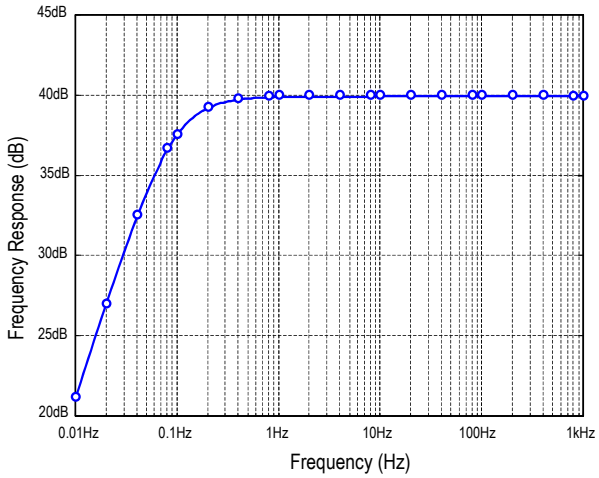

Fig. 4. Differential gain A_{DD} frequency response of the built prototype. The A_{DD} predicted by (11) for the components values in (30) is shown in solid line and experimental data with markers.

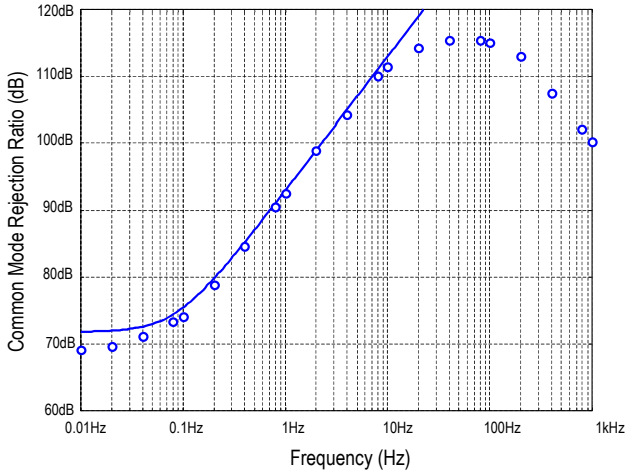

Fig. 5. Common Mode Rejection ratio of the FD prototype. The *CMRR* regarding only the first term in (32) is shown in solid line. This curve agrees with experimental data (in markers) for low frequencies; then the effect of OA's CMRR unbalances becomes dominant and the *CMRR* decays.

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