A Fully-Differential DC Restoration Circuit

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Abstract—Modern instrumentation is moving towards fully differential conditioning circuits. They provide an elegant and efficient way to adapt differential signals, like those provided by balanced sensors, to differential-input analog-to-digital converters (ADC). For that to be possible, many well-known Single-Ended (SE) conditioning circuits must be converted to their Fully-Differential (FD) versions. This work presents a FD dc servo circuit, able to restore both common mode and differential mode dc levels to their desirable values, suited to those required by the ADC to optimize its input range. The general scheme and the design procedure to adapt the circuit to particular needs are presented. Also experimental data obtained from a FD dc restoration circuit are presented.

Keywords—fully-differential circuit; dc restoration; dc servo amplifier; common mode rejection ratio.

I. INTRODUCTION

DC restoration is a usual analog processing task, often used to reject signal dc components and amplifier offset voltages, ensuring a dc baseline level that allows fully exploiting the input range of analog stages or ADCs. This technique rejects unknown and variable dc components to establish a proper dc level. A general scheme of this kind of circuit is shown in Fig. 1 (a). The circuit output \( V_o \) is compared with the desired dc value (\( V_{REF} \)), the difference is integrated and feedback to the input. By this way, the dc output level equals to \( V_{REF} \) and the resulting transfer function is:

\[
T(s) = \frac{1}{1 + s \cdot \tau_i/G} \tag{1}
\]

The more usual circuit is based on an inverter amplifier topology [1], it presents low input impedance and is not appropriate for front-ends, which generally require high input impedances. A single-ended (SE) dc restoration topology based on the non-inverter topology (high input impedance) is presented in Fig. 1 (b) [2].

Single-ended conditioning circuits are suited for unbalanced sensors, but not for balanced ones, like bridge sensors, that provide differential outputs. A common solution is to convert the differential signal to SE using a differential amplifier, and then process by SE circuits (i.e. restoring dc levels). Furthermore, current high resolution ADCs have differential inputs, requiring to reconvert the processed SE signals to differential mode again, before being connected to the ADC. These multiple conversions inevitably lead to signal degradation and also to a reduction of the dynamic range [3].

A natural and well-suited alternative is to use FD circuits for conditioning differential output sensors to differential input ADCs [4]. Moreover, FD circuits have higher dynamic range than their SE counterparts; they are ideally insensitive to variations on ground potential along the printed circuit board traces, and are well-suited to manage bipolar voltages by single voltage power-supplies (among other advantages). These are some of the reasons why instrumentation circuits trend is moving toward fully-differential topologies.

Fig. 1. (a) General scheme of a dc restoration circuit and (b) a Single-Ended circuit that implements it.

Fully-Differential circuits work with both Differential Mode (DM) and Common Mode (CM) voltages. When DM (\( v_{ID} \)) and CM (\( v_{IC} \)) voltages are applied to the input, DM (\( v_{OD} \)) and CM (\( v_{OC} \)) voltages appear at the output. Differential \( v_{ID} \) and common mode voltages \( v_{IC} \) are defined in terms of ground-referenced voltages \( v_H \), \( v_L \) at the circuit’s nodes by:

\[
v_{ID} = v_H - v_L ; \quad v_{IC} = 0.5(v_H + v_L) \tag{2}
\]

The input-output voltage relationship can be expressed as:
\[ v_{ad} = G_{DD} v_{id} + G_{DC} v_{ic}, \]
\[ v_{dc} = G_{CD} v_{id} + G_{CC} v_{ic}, \]

where \( G_{DD} \) represents the DM gain and \( G_{CC} \) the CM gain [5]. Expression (3) can be presented in a more compact form denoting differential and common mode voltages as components of a voltage vector (in capital letters):

\[ V = G \cdot V_i \]

(4)

The cross-terms \( G_{DC} \) and \( G_{CD} \), related to mode’s transformations, are ideally zero, but in practice they have non-null values due to component unbalances. The main merit factor for FD circuits is the well-known Common Mode Rejection Ratio (CMRR) defined as:

\[ CMRR = \frac{G_{dd}}{G_{dc}} \]

(5)

Avoiding grounded elements it is possible to design FD circuits for ultra high CMRR [6], but this approach leads to a unity \( G_{CC} \) and is not feasible to conditioning CM voltages, which are ground-referred potentials. This work presents a FD circuit that implements the scheme of Fig. 1(a). It processes DM and CM voltages, thus allowing to restore dc levels for both modes.

II. PROPOSED CIRCUIT

The proposed circuit, presented in Fig. 2, is a fully-differential version of that in Fig. 1(b), which was adopted as starting SE prototype. This FD topology was obtained by mirroring and coupling the SE prototype according to [6].

Fig. 2. Proposed circuit for dual mode dc restoring. It sets at its output \( V_{DREF} \) and \( V_{CREF} \) dc levels for DM and CM respectively.

The circuit can be decomposed in a FD difference amplifier \( G \) and a FD feedback network \( H \) connected as indicated in the circuit of Fig. 2. Figure 3 shows the same idea but in a schematic form.

The amplifier \( G \) has two inputs \( V_i \), \( V_{FB} \) and one output \( V_o \). Its input-output relationship can be expressed as:

\[ V_o = [G_1 \ G_2] \begin{bmatrix} V_i \\ V_{FB} \end{bmatrix}, \]

(6)

where the matrix gain elements are given by:

\[ G_{DD1} \equiv 1 + \frac{2 \cdot R_2}{R_1 / 2 R_3} ; \quad G_{DC1} = \frac{1}{2} \left( \frac{R_1}{2 R_3} - \frac{R_2}{2 R_2} + \frac{R_2 - R_1}{R_3} \right) \]

(7)

\[ G_{DD2} = - \frac{R_2}{R_1} ; \quad G_{DC2} = - \frac{R_3}{2 R_3} \]

and \( R_i \) denotes the average value of component \( R_i \).

Fig. 3. Proposed circuit as interconnected matrix gain building blocks.

The feedback circuit (see Fig. 2) presents a pole at the origin and provides the AC coupling feature to the composed amplifier. This circuit is FD and the elements of its matrix gain \( H \) are given by:

\[ H_{DD} \equiv 1 + \frac{1}{s R C_i} ; \quad H_{DC} = \frac{1}{s} \left( \frac{1}{R C_i} - \frac{1}{R C_i'} \right) \]

(8)

\[ H_{CC} \equiv 1 + \frac{1}{s R C_i} ; \quad H_{CD} = \frac{1}{4s} \left( \frac{1}{R C_i} - \frac{1}{R C_i'} \right) \]

A. Differential Mode Gain

Solving the scheme of Fig. 3 for differential mode voltages results in:

\[ v_{ad} = v_{id} G_{DD1} + v_{FB} G_{DD2} \]
\[ v_{FB} = v_{ad} H_{DD} \]

(9)

and the DM gain \( A_{DD} \):

\[ A_{DD} = \frac{v_{ad}}{v_{id}} = \frac{G_{DD1}}{1 - G_{DD2} H_{DD}} \]

(10)

Replacing the expressions of \( G_{DD1}, G_{DD2} \) and \( H_{DD} \) (7), (8):
\[ A_{\text{dd}} = \frac{A_{\text{dd}} \tau_s}{1 + s \tau} \]  

(11)

where:

\[ A_{\text{dd}} = 1 + 2 \frac{R_2}{R_1} \]  

(12)

**B. Common Mode Gain**

By a similar procedure, the CM mode gain \( A_{\text{cc}} \) results:

\[ A_{\text{cc}} = \frac{v_{\text{oc}}}{v_{\text{cc}}} = \frac{G_{\text{cc1}}}{1 - G_{\text{cc2}} H_{\text{cc}}} \]  

(13)

\[ A_{\text{cc}} = \frac{\tau_s}{1 + \tau_s} \]  

(14)

**C. Common Mode Rejection Ratio.**

In order to find the overall CMRR, as a first step the CM-to-DM Gain \( A_{\text{dc}} \) must be calculated. If a common mode voltage \( v_{\text{cc}} \) is applied to the amplifier input, neglecting second order effects as double conversion factors, the differential and common mode output voltages \( (v_{\text{od}}, v_{\text{oc}}) \), are:

\[ v_{\text{od}} = v_{\text{cc}} G_{\text{dc1}} + v_{\text{od}} H_{\text{dd}} G_{\text{dd2}} + v_{\text{oc}} \left( \frac{H_{\text{cc}} G_{\text{dc2}}}{H_{\text{dc}} G_{\text{dd2}}} \right) \]  

(15)

\[ v_{\text{oc}} = v_{\text{cc}} G_{\text{cc1}} + v_{\text{oc}} G_{\text{cc3}} G_{\text{cc2}} \]  

(16)

Solving \( v_{\text{cc}} \) from (16), replacing it in (15), and using that \( G_{\text{cc2}}=G_{\text{dd2}}, H_{\text{cc}}=H_{\text{dd}}, G_{\text{dc2}}=-G_{\text{dc1}} \) and \( G_{\text{dd2}}=G_{\text{cc1}}=1 \), the gain \( A_{\text{dc}} \) results:

\[ A_{\text{dc}} = \frac{G_{\text{dc1}}}{\left(1 - \frac{H_{\text{dd}} G_{\text{dd2}}}{H_{\text{dc}} G_{\text{dd2}}} \right)} \]  

(17)

Replacing (7) and (8) in (17):

\[ A_{\text{dc}} = \frac{v_{\text{od}}}{v_{\text{oc}}} = A_{\text{dc0}} \cdot \frac{s}{1 + s \tau} \]  

(18)

with

\[ A_{\text{dc0}} = - \left[ \left(1 - \frac{R_2}{R_2} \right) + \left(1 + \frac{R_2}{R_1} \right) \left(1 - \frac{R_1}{R_2} \right) \right] \frac{R_0 R_2}{R_2} \]  

(19)

Assuming resistors and capacitors with tolerances \( t_R \) and \( t_C \) respectively, the maximum value of \( A_{\text{dc0}} \) (worst case) is given by:

\[ A_{\text{dc0}} \leq 2 \tau \left(t_R \left(\frac{R_2}{R_1} + 3 \frac{R_2}{R_1}\right) + t_C \right) \]  

(20)

Expression (18) only considers passive component unbalances. Adding the effects of finite CMRR operational amplifiers (OA), it becomes:

\[ A_{\text{dc}} = A_{\text{dc0}} \cdot \frac{s}{1 + s \tau} + \left( \frac{1}{\text{CMRR}_{A1}} - \frac{1}{\text{CMRR}_{A2}} \right) A_{\text{dd}} \]  

(21)

where \( \text{CMRR}_{A1} \) denotes the common mode rejection ratio of the OA composing the front-end amplifier \( G \). Finally, from (11) and (18) it is possible to find the overall CMRR:

\[ \text{CMRR}^{-1} = \frac{A_{\text{dc0}}}{A_{\text{dd}}} \cdot \frac{1}{1 + s \tau} + \frac{1}{\text{CMRR}_{A1}} - \frac{1}{\text{CMRR}_{A2}} \]  

(22)

**D. Differential DC input Range**

An important feature of a dc restoring system is its dc input range. This means the maximum dc level at the input that the circuit could manage and reject. The differential output voltage \( v_{\text{od}} \) of the input amplifier \( A \) can be expressed as a function of the DM voltage of its two inputs \( v_{\text{DD}}, v_{\text{FD}} \) as:

\[ v_{\text{od}} = v_{\text{DD}} G_{\text{DD1}} + v_{\text{FD}} G_{\text{DD2}} \]  

(23)

In the limit of the range of operation, \( v_{\text{FD}} \) takes the maximum possible differential voltage \( v_{\text{DD}} = \pm(V_{\text{cc}} - V_{\text{DD}}) \), while \( v_{\text{DD}} = 0 \). Then, as the dc suppression system is working, it corrects the output voltage to \( v_{\text{od}} = 0 \). In this situation, (22) becomes:

\[ 0 = v_{\text{DD}} G_{\text{DD1}} + (V_{\text{cc}} - V_{\text{DD}}) G_{\text{DD2}} \]  

(24)

and the maximum admissible \( v_{\text{DD}} \) results in:

\[ v_{\text{DD}} = \pm (V_{\text{cc}} - V_{\text{DD}}) G_{\text{DD2}} \]  

(25)

Using (7) and (12), it is possible to express \( v_{\text{DD}} \) as a function of the nominal differential gain \( A_{\text{dd}} \) and the \( R_1/R_2 \) ratio as:

\[ v_{\text{DD}} = \pm \left( V_{\text{cc}} - V_{\text{DD}} \right) A_{\text{dd}} \]  

(26)

**E. Design example**

As a design example, an amplifier with gain \( A_{\text{dd}}=100 \), dc input range of \( \pm120 \text{mV} \), \( V_{\text{cc}}=12 \text{V} \), \( V_{\text{DD}}=12 \text{V} \) and cutoff frequency lower than 0.1 Hz, will be described. Given the dc input range \( V_{\text{iddc}} \) and the nominal gain \( A_{\text{dd}} \), the \( R_1/R_2 \) ratio can be found from (25) as:

\[ R_1/R_2 = \frac{(V_{\text{cc}} - V_{\text{DD}})}{V_{\text{iddc}}} \cdot A_{\text{dd}} \]  

(27)

Then, the ratio \( R_2/R_1 \) can be obtained from (12):

\[ R_2/R_1 = 0.5 \left( 1 + R_2/R_1 \right) \left( A_{\text{dd}} - 1 \right) \equiv 100 \]  

These resistor relationships can be fulfilled, for example, with \( R_2=220 \text{k} \Omega, R_1=220 \text{k} \Omega, R_1=2200 \text{k} \Omega \). Finally, to achieve the cutoff frequency of 0.1 Hz (\( \tau=1.6 \text{s} \)), according to (12):

\[ C = \frac{1 + R_1/R_2}{1} = 1.6 \text{s} \]  

(28)

that for \( R_3/R_2=1 \) results in:

\[ R_3 = 0.8 \text{ s} \]  

(29)

In order to provide a margin for component tolerances, the values \( R_1=820 \text{k} \Omega, C_1=1 \mu F \) were adopted, resulting a nominal cutoff frequency slightly lower than 0.1 Hz. Finally, the
component values are: $R_1=2.2\, \text{k}\Omega$, $R_2=220\, \text{k}\Omega$, $R_3=220\, \text{k}\Omega$, $R_i=820\, \text{k}\Omega$, $C_i=1\, \mu\text{F}$.

**F. Experimental validation**

The circuit was built using 2% tolerance resistors, 10% tolerance capacitors, and general-purpose LF353 OAs. No selection was made and the component values were:

\[
C_i=1.15\mu\text{F}, \quad C_i'=1.12\mu\text{F}, \quad R_i=816.5\, \text{k}\Omega, \\
R_i'=809.4\, \text{k}\Omega, \quad R_2=218.0\, \text{k}\Omega, \quad R_3=215.4\, \text{k}\Omega, \\
R_1=214.2\, \text{k}\Omega, \quad R_1'=215.3\, \text{k}\Omega, \quad R_2=2202\, \Omega.
\]

According to (11), (14) y (21), the main amplifier transfer functions $A_{DD}$, $A_{CC}$ and its $CMRR$ are:

\[
A_{DD} = \frac{v_{SD}}{v_{ID}} = \frac{182.1s}{1+s1.84}, \quad A_{CC} = \frac{1.84s}{1+s1.84}, \quad CMRR = \frac{1}{1+s\tau} + \frac{1}{CMRR_1} \cdot \frac{CMRR_2}{CMRR_1}
\]  

In Fig. 7, the differential $A_{DD}$ gain given by (31) and the measured data are shown. Finally, Fig. 8 shows the experimentally obtained $CMRR$. Both experimental results show a good agreement with those predicted by expressions (31) and (32).

**III. CONCLUSIONS**

An FD circuit that restores dc level for both differential mode and common mode voltages was proposed. It allows setting proper dc voltages to fully exploit the input range of current differential input ADCs. Its $CMRR$ is moderate at low frequencies (around 70 dB), but increases up to 110 dB for higher frequencies, where it is limited by operational amplifiers $CMRR$ unbalances.

There is a trade-off between $CMRR$ and dc input range. Reducing resistor $R_1$ value increases differential mode gain $A_{DD}$ and $CMRR$, but reduces the maximum dc input range. Analytic design equations were provided and experimentally validated.

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