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Double-Differential Amplifier for sEMG Measurement by Means of a Current-Mode Approach

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ABSTRACT This work proposes a Double Differential (DD) amplifier topology which exploits the advantages of the current-mode approach. DD amplifiers are useful as front-ends in standalone active electrodes for superficial electromyography (sEMG) wearable applications and electroneurography (ENG) measurement devices. Front-ends for these applications need to attain low noise, high common-mode rejection ratio, and high input impedance to measure biopotential signals and can further benefit from low power operation, a small size, and an easily adaptable output. Presently published DD amplifiers are either complex in terms of a high part count, leading to higher power consumption and size, or suffer from limited interference-rejection capabilities and require further analog processing for compatibility with single-ended systems. Therefore, in this work, second-generation current conveyors have been leveraged to obtain a simple topology combining a small active-part count, a high common-mode rejection ratio, and a flexible output stage. The current-mode DD amplifier is presented and analyzed in detail to estimate its parameters and model the effects of nonidealities in the circuit. In order to validate the proposed topology, a discrete-component implementation was realized as a proof-of-concept. The results experimentally demonstrated the properties of the proposed topology and its feasibility for measuring superficial sEMG DD signals.

INDEX TERMS Active electrode, amplifier, biopotential instrumentation, current conveyor, double-differential, electromyography.

I. INTRODUCTION

Double differential (DD) electrodes are useful in superficial electromyography (sEMG) because they help to reject crosstalk from muscles outside the volume of interest, as DD configurations have increased spatial selectivity compared with differential (i.e. bipolar) ones [1], [2]. A DD electrode (also known as *Linear* DD electrode) has 3 contacts, evenly spaced along a line, that measure voltages v_a, v_b, and v_c respectively as depicted in Fig. 1, and perform the following operation to obtain the DD output:

$$v_{DD} = v_a - 2\,v_b + v_c \tag{1}$$

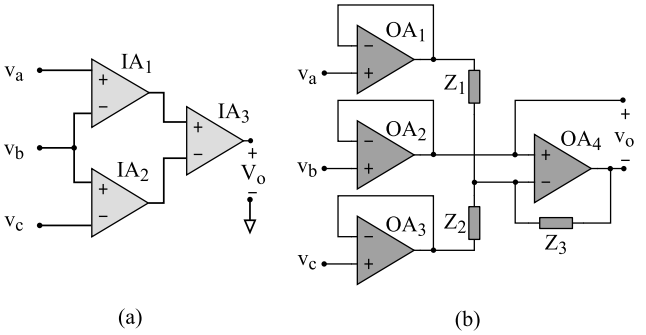

FIGURE 1. DD active electrode implementations from the literature based on voltage-mode devices.

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sEMG electrodes are employed in wearable devices using large numbers of sensors distributed throughout the body.

These sensors may be implemented as small standalone wireless systems in each measurement location (e.g. the DD Trigno EMG from Deslys [3], or the differential FREEEMG form BTS Bioengineering [4]) requiring low power consumption, or as active electrodes transmitting the signal from each sensor to a central device on the body by wires (Thalmic Labs Myo Armband [5], Ottobock Myo Plus TR [6]), requiring a robust and simple signal distribution strategy [7]. In both cases, the sensors must be small and lightweight for patient comfort and to avoid artifacts [8], and they require good electromagnetic interference rejection capabilities.

Wearable and implantable devices implement sensors in application-specific integrated circuits (ASICs) which include an analog front-end, digitization, and data processing and transmission in a single IC with no or few external components [9]. This has enabled ultra-low-power arrays and single-electrodes suited for EMG and electroneurogram (ENG) recordings to be implemented, which rely on a low-noise biopotential readout analog front-end to measure the target signal rejecting interference sources [10]–[14]. In these cases, new topologies that optimize the trade-off between required area, power consumption, and performance are desirable. ENG electrodes, in particular, have leveraged integrated DD front-ends [15], [16].

There are currently two published alternatives to evaluate the exact DD output, see Fig. 1. The traditional topology amplifier in Fig. 1a finds v_{DD} in relationship (1) by using 3 instrumentation amplifiers (IAs). It attains an excellent common-mode rejection ratio (CMRR) that depends on the imbalances between the CMRR of each IA. However, firstly, it is a complex circuit in terms of the required active components or blocks, since each IA is generally implemented by 3 operational amplifiers (OAs), for a total of 9 OAs. Secondly, the CMRR is not the only determining factor for interference rejection: the potential-divider effect [17] produces a common-mode to differential-mode transformation at the input of the amplifier due to the finite and unbalanced input and electrode impedances. Although input impedances are large, determined by capacitances of the order of 1-10pF, it was shown that the imbalanced input of the 3 IA topology renders its high CMRR ineffective [18] when large electrode impedances are present, as can occur with small EMG electrodes [2].

The second alternative is the much simpler implementation based on 4 OAs, shown in Fig. 1b and proposed in [18]. It, with a reduced number of active components, solved the input imbalance problem. However, its CMRR is limited not only by the imbalance of the first-stage OAs but also by the absolute CMRR of OA_4 and further by its open-loop gain [18]. In addition, this implementation presents a voltage-mode differential output, but this kind of output is only convenient when interfacing with voltage-mode differential-input stages; otherwise, an additional mode-transformation circuit is required.

In order to develop a topology to evaluate v_{DD} without the complexity of the topology in Fig. 1a, but improving the CMRR drawback of the topology in Fig. 1b, in this paper the current-mode approach is explored [19], [20]. Indeed, we take inspiration from [21], where Toumazou & Lidgey proposed both an IA, which is traditionally designed following the voltage-mode approach, but by using a current-mode approach, and a simpler circuit trading off performance for simplicity. That concept proved attractive for biopotential measurements [22], [23] and was used in an improved implementation achieving a higher CMRR [24].

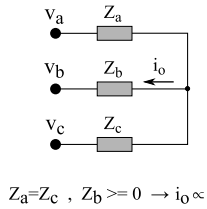

FIGURE 2. Calculation of the DD output through an impedance network.

Some variations of current-mode IAs arose thanks to the possibility of improving several parameters such as frequency performance, circuit simplicity, and low-voltage operation [25, p. V]. Furthermore, a current-output topology can help distribute the signal when the active electrodes are wired and offer robustness against voltage-mode interference [26], [27].

In particular, in this paper, a novel simple topology to obtain the DD output is presented. It exploits the use of a second-generation current conveyor (CCII) [28], and despite its simplicity, thanks to its balanced topology, as suggested by previous work on current-mode IAs, can provide a high CMRR even accounting for the CCII non-idealities. The solution is also suited to be realized in an integrated version as an analog front-end for acquisition ASICs. To validate the idea, in the paper the topology is fully analyzed including circuit non-idealities, and experimental measurements have been carried out on a discrete board-level implementation. The goal of the experimental measurements is to prove that the model and derived equations are valid and that all significant non-idealities that could hinder the front-end's instrumentation capabilities have been identified.

The paper is structured as follows. In Section II after a brief introduction to the CCII, the current-mode DD amplifier topology is presented and discussed. In Section III, the proposed topology is analyzed in detail and a model which accounts for non-ideal parameters is also included. In Section IV simulation and experimental validation are reported. In particular, a discrete-component implementation as a proof-of-concept device and DD sEMG signals obtained from experimental in-vivo measurements are included. Finally, the conclusions are drawn in Section V.

II. PROPOSED DD ELECTRODE TOPOLOGY

A. DD CALCULATION

The proposed topology is based on the impedance network shown in Fig. 2, which by itself can calculate the DD output if the current through Z_b can be measured. Using the nomenclature displayed in Fig. 2, the impedance network produces

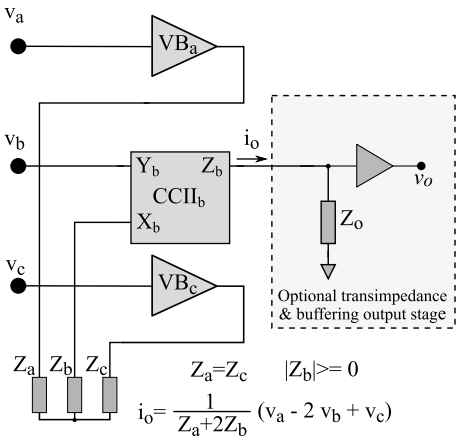

FIGURE 3. Proposed topology. A CCII device is used to obtain i_o while voltage buffers $VB_{a,c}$ help implement a high-impedance, balanced input stage.

a current i_o equal to

$$i_o = \frac{v_a}{Z_a + Z_{b||c}} \frac{Z_{b||c}}{Z_b} - \frac{v_b}{Z_b + Z_{a||c}} + \frac{v_c}{Z_c + Z_{a||b}} \frac{Z_{a||b}}{Z_b} \tag{2}$$

$$= \frac{1}{Z_b Z_a + Z_b Z_c + Z_a Z_c} \left(Z_c v_a - (Z_a + Z_c) v_b + Z_a v_c\right), \tag{3}$$

where $Z_{x||y}$ denotes the parallel combination of Z_x and Z_y.

If $Z_a = Z_c$ the double differential output is obtained:

$$i_o = \frac{1}{Z_a + 2Z_b}(v_a - 2v_b + v_c) = \frac{1}{Z_a + 2Z_b} v_{DD}, \tag{4}$$

where Z_a was used in this simplified expression for both Z_a and Z_c under the assumption that they are equal.

This method has two important properties:

- The CM is rejected by the first stage because it is not present in the output current signal.
- Although it is based on passive components that must have equal values, the effect of imbalances notably neither affects the correct calculation of the DD output nor introduces significant mode transformations

Concerning the last point, the imbalances in Z_{a-c} do not degrade the CMRR and only impact the rejection of EMG crosstalk, as will be considered in detail in section III-B. Therefore, the DD signal can be obtained with this simple topology by only measuring the current i_o.

B. CCII

In order to measure the current i_o in the network of Fig. 2, a Current Conveyor (CC) can be used. The CC is an electronic building block originally introduced in 1968 by Smith and Sedra [29]. To improve its versatility, the same authors two years later proposed a second-generation CC (CCII) [28], which for its characteristic can find useful and more concrete applications in the electronic analog domain. The ideal CCII is a three-terminal device whose nodes, labeled with X, Y and Z, have the following electrical relationship:

$$\begin{bmatrix} v_x \\ i_y \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_x \\ v_y \\ v_z \end{bmatrix} \tag{5}$$

where the + and - signs in the matrix are used for positive (CCII+) and negative type (CCII−) conveyors, respectively.

By inspection of matrix (5), a CCII can be thought of as composed of a voltage follower between Y and X nodes, and a positive (CCII+) or a negative (CCII−) current follower, since the current on node Z replicates the current flowing through X.

C. DD AMPLIFIER DESIGN

The proposed DD amplifier, reported in Fig. 3, is based on the floating impedance network from Fig. 2 capable of performing the DD signal calculation given by (1) with ideally infinite CMRR. First, each electrode signal must be buffered to present a balanced, high-impedance input stage, and the current through the central electrode's impedance must be measured using a CCII− device.

Following Fig. 3 the output current is

$$i_o = \frac{1}{Z_a + 2Z_b} v_{DD}. \tag{6}$$

Current i_o can be converted to voltage so it can be fed to traditional voltage-input devices, or it can be further processed in current-mode circuits. Here we will include the transimpedance stage for compatibility with the board-level proof-of-concept to be built. The negative CCII device was chosen to obtain a positive v_{DD} voltage as defined in (1) at the output. The impedance used to convert the current output to a voltage output can also be useful for filtering purposes.

III. TOPOLOGY ANALYSIS

The DD amplifier is quite different from a traditional differential amplifier, and its performance parameters must be defined in order to study it. Previous work [18] presented a framework to analyze DD amplifiers. The common mode, differential mode, and double differential mode were identified as signal modes useful for analysis. They are defined by the following transformation matrix:

$$\begin{bmatrix} v_{DDM} \\ v_{CM} \\ v_{DM} \end{bmatrix} = \begin{bmatrix} 1 & -2 & 1 \\ 1/3 & 1/3 & 1/3 \\ 1 & 0 & -1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{7}$$

Thus, given a single-ended output v_o three gains can be defined, omitting frequency dependency for simplicity:

$$v_o = G_{DD} v_{DDM} + G_D v_{DM} + G_C v_{CM} \tag{8}$$

The mode of interest for the system is the DD signal, v_{DDM}, whereas v_{CM} and v_{DM} should be rejected. The capability of the amplifier to reject these signals can be described by its $CMRR := G_{DD}/G_C$ and its differential mode rejection ratio or $DMRR := G_{DD}/G_D$. Interference can get into the system if the CMRR is not high enough (over 80 dB [30]).

In a biopotential measurement system, a CM voltage rejection circuit known as Driven Right Leg (DRL) can help to provide 30-60 dB of this rejection and the rest must be provided by the input stage of the front-end. Moreover, muscular crosstalk can also affect measurements if the DMRR is not high enough (over 40 dB).

For generality, a single-ended output voltage v_o will be considered, given by the product of a transimpedance gain R_T times the output current i_o. The output current itself can be obtained as the superposition of all modes following (8) by defining transconductance gains $G_{i,x}$ where x stands for each mode, so that

$$v_o = R_T\, i_o \tag{9}$$

$$= R_T \left(G_{i,DD}\, v_{DDM} + G_{i,D}\, v_{DM} + G_{i,CM}\, v_{CM}\right) \tag{10}$$

Hence for the proposed topology, from (6):

$$G_{i,DD} = \frac{1}{Z_a + 2Z_b} \tag{11}$$

In order to analyze factors degrading the performance of the presented topology, CCII devices will be represented including nonidealities according to the following simplified model [31]:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} Y_y & 0 & 0 \\ A_{vf} & Z_x & 0 \\ G_{mf} & A_{if} & Y_z \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{12}$$

Reverse effects have been considered negligible. Impedances at the terminals have been included, as well as the forward voltage and current gains. Frequency dependency has been omitted for simplicity. The forward transconductance from terminal Y_b to Z_b has also been included as an important nonideality with an important impact on the CMRR. The same parameters that describe the voltage buffer of the CCII device can be used to describe VB_a and VB_c to avoid the proliferation of notation.

Using this model, which accounts for nonidealities, the proposed active electrode is shown in Fig. 4, where the parasitic impedance of the common node v_n to ground has been added as well since it is an important parameter for the calculation of the CMRR.

A. COMMON-MODE REJECTION

The proposed topology has the potential to achieve a high CMRR because the CM is rejected by the first stage. The DD signal analog calculation is performed by the impedance network Z_{a-c} and as it is a "floating" network, i.e. it has no paths to ground, its CMRR is ideally infinite [32]. Nonidealities, however, will have an impact on the CMRR, as listed in the following subitems.

1) INPUT IMPEDANCE

The imbalance of input admittances $Y_{Y_a}, Y_{Y_b}, Y_{Y_c}$ can degrade the CMRR when electrode impedance reaches a high value (above 1 MΩ), as shown in previous work in [18]. High impedance values of the order of 1 MΩ and above can result

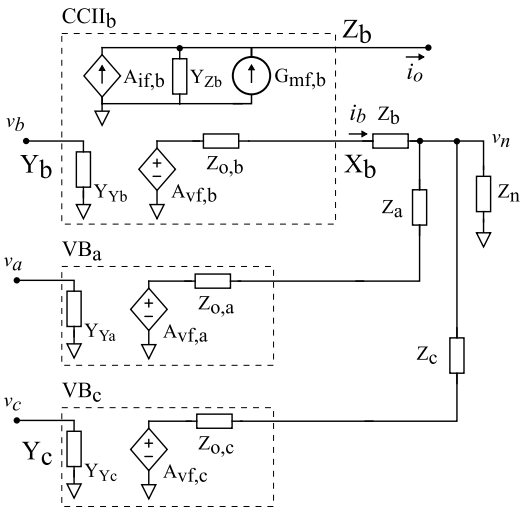

FIGURE 4. Model of the proposed DD amplifier including CCII parameters and parasitic impedance Z_n.

when using small Ag/AgCl electrodes of 5 mm^2 on unprepared skin [33]. Because the input is balanced in the topology hereby presented, this effect can be made negligible with implementations achieving current commercial standards of the order of 1-10 pF [18], considering that at interference frequencies (50/60 Hz and the first 5 harmonics) the capacitive component is strongly dominant in CMOS implementations.

2) PARASITIC IMPEDANCE ON THE FLOATING AVERAGING NODE

When the parasitic impedance Z_n on the v_n node is not infinite, a CM current can circulate to ground through impedances Z_{a-c} and degrade the CMRR producing a CM transconductance gain equal to:

$$G_{i,CM} = \frac{i_o}{v_{CM}} = \frac{1}{Z_b} \frac{1}{1 + Z_n/Z_{a||b||c}} \tag{13}$$

For the simple case of all impedances being resistances of equal value, ($R_{a||b||c} = R_b/3$), and Z_n considered as a parallel of C_n and R_n, replacing in (13) we get

$$G_{i,CM} = \frac{1}{3R_n} \frac{(1 + sR_nC_n)}{(1 + sR_bC_n/3)}, \tag{14}$$

yielding a CMRR due to v_n parasitic impedance equal to

$$CMRR_{vn} = \frac{G_{i,DDM}}{G_{i,CM}} = \frac{R_n}{R_b} \frac{(1 + sR_bC_n/3)}{(1 + sR_nC_n)} \tag{15}$$

under the same set of conditions. For example, if $R_b = 10\,\text{k}\Omega$, even with a very high R_n, a $C_n = 1$ pF would yield a CMRR limit of 110 dB.

3) FORWARD TRANSCONDUCTANCE

The effect of G_{mf} will be considered, as it is usually an important factor that degrades CMRR in CCII devices [31]. Setting all inputs as v_{CM} the circuit from Fig. 4 yields

$$i_o = G_{mf,b}\, v_{CM},$$

thus, with the nomenclature from (10)

$$G_{i,CM} = G_{mf,b} \tag{16}$$

and the CMRR due to G_{mf} results

$$CMRR_{G_{mf}} = \frac{1}{(Z_a + 2Z_b)G_{mf,b}}. \tag{17}$$

Therefore, for example, with $Z_a = Z_b = Z_c = 10\,\text{k}\Omega$, the $G_{mf,b}$ should be below $-170\,\text{dB}$ to preserve a 90 dB CMRR,.

4) ACTIVE PARAMETERS IMBALANCE

Active gains $A_{vf,a-c}$ can also degrade the CMRR if imbalanced. When v_{CM} is applied to all inputs the voltage at each X terminal is $v_{CM}A_{vf}$, the current output is

$$i_o = v_{CM}\frac{\left(A_{vf,a} - 2A_{vf,b} + A_{vf,c}\right)}{Z_a + 2Z_b}, \tag{18}$$

which using (11) yields

$$CMRR_{A_{vf}} = \frac{1}{A_{vf,a} - 2A_{vf,b} + A_{vf,c}}. \tag{19}$$

Note that $A_{vf} \approx 1$, usually resulting from closed-loop active circuits, hence achieving very small imbalances and in turn a high overall CMRR limit.

B. DIFFERENTIAL MODE REJECTION

Because the signal of interest is the DDM, the DM represents an interference signal and it should be rejected. (3) can be rewritten as:

$$i_o = \varphi(Z_c v_a - (Z_a + Z_c)v_b + Z_a v_c), \tag{20}$$

where φ stands for $1/(Z_bZ_a + Z_bZ_c + Z_aZ_c)$ for simplicity. Considering $Z_a \neq Z_c$ the value of these resistors can be rewritten as $Z_a = Z - \Delta Z; Z_c = Z + \Delta Z$. Therefore, replacing in (20)

$$\begin{aligned} i_o &= \varphi\left((Z + \Delta Z)v_a - 2Zv_b + (Z - \Delta Z)v_c\right) \\ &= \varphi Z v_{DD} + \varphi \Delta Z v_D \end{aligned} \tag{21}$$

Yielding:

$$\begin{aligned} G_{i,DD} &= \varphi Z, \\ G_{i,D} &= \varphi \Delta Z, \\ DMRR &= G_{i,DD}/G_{i,D} = Z/\Delta Z. \end{aligned} \tag{22}$$

The differential-mode signal is an EMG signal, of the same order of magnitude as the DD signal. Hence with resistor tolerances below 1 %, the DMRR is high enough.

C. NOISE ANALYSIS

Next, e and i_n will be used to symbolize amplitude spectral densities (in $\text{V}/\sqrt{\text{Hz}}$ and $\text{A}/\sqrt{\text{Hz}}$ respectively). The total current noise at the output of the first stage of the topology (the Z_b terminal), $i_{n,o}$, has contributions from the voltage noise sources referred to each CCII Y-terminal e_Y, which will be denoted $i_{n,o|e_Y}$, and the thermal noise from the resistive component of the impedances e_R, denoted $i_{n,o|e_R}$. Hence

$$i_{n,o}^2 = i_{n,o|e_Y}^2 + i_{n,o|e_R}^2. \tag{23}$$

Assuming that CCIIa and CCIIc devices have the same noise ($e_{Y_a} = e_{Y_c}$) then

$$i_{n,o|e_Y}^2 = 2\left(\frac{e_{Y_a}}{Z_a + Z_b + Z_c}\right)^2 + \left(\frac{e_{Y_b}}{Z_b + Z_a||Z_c}\right)^2 \tag{24}$$

Because of the Y-to-X voltage buffer, each device's voltage noise e_Y appears in series with its corresponding resistor's voltage noise e_R, hence $i_{n,o|e_R}$ can be found directly replacing e_Y for e_R in (24).

If the transimpedance stage is considered, the total output noise voltage of the system is

$$e_o^2 = (i_{n,o}R_T)^2 + e_{R_T}^2, \tag{25}$$

where R_T is the transfer function of the second stage defined in (9), and e_{R_T} is the total noise contribution from the same stage.

Finally, when used in biomedical applications, the current noise sources of Y-terminals are important as well because they produce a voltage across electrode impedances.

D. DC PARAMETERS

If $Z_{a,b,c}$ are selected as resistors for DC-coupled measurements and R_T is implemented, the gain of this stage will be limited by the large DC offset of the biopotential measurement electrodes, $V_{E,a-b-c}$, of up to $\pm 150\,\text{mV}$. Considering a worst-case with $V_{E,a} = V_{E,c} = -V_{E,b}$, then $i_o = \pm 4V_E/(2R_a + R_b)$ and in a system with supply V_s, R_T should be designed so that, at least, $G_{DD} < V_s/(4V_E)$. This is valid for any DD topology.

The offset voltage of each active device can be represented in series with the electrode offset, therefore presenting a negligible effect compared to the requirement of conforming to this offset. Input bias currents must be low enough to avoid surpassing the limits required by electrical safety standards for biopotential measurement devices [34].

Further, input bias currents I_b transverse the electrodes' impedances Z_E and could produce a problematic voltage drop. A simple rule is that this drop should not exceed one order of magnitude below the electrode offset: $I_bZ_E < 10\,\text{mV}$, for example, 10 nA maximum for 1 MΩ. Electrodes of smaller size and factors such as dry skin can result in higher impedances, lowering the admissible bias current. For very high values, specialized CMOS input stages can attain low bias currents even in commercial components (e.g. 20 fA for Texas Instruments' LMP7721). Otherwise, AC-coupling could be implemented in the presented topology by including a DC-blocking capacitor in Z_b as will be discussed in Sec. IV-D.

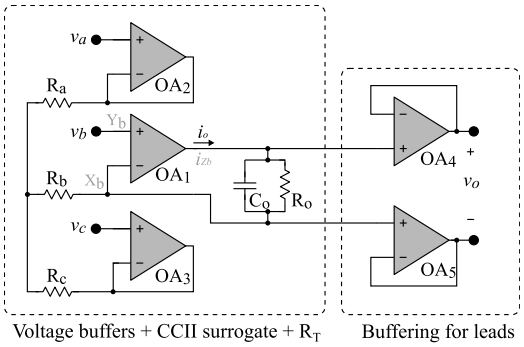

FIGURE 5. A proof-of-concept implementation with the purpose of validating the proposed topology.

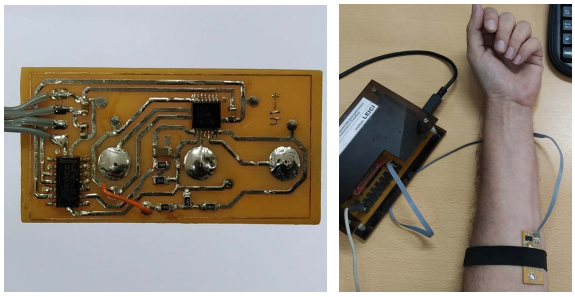

FIGURE 6. Photographs of the amplifier built as a sEMG active electrode (a), and the EMG measurement setup (b).

IV. EXPERIMENTAL RESULTS AND VALIDATION

A. DISCRETE PROOF-OF-CONCEPT DESIGN

A proof-of-concept circuit was implemented with the goal of validating the topology in a real-world measurement setup and verifying the design equations.

The proposed topology was implemented using the circuit from Fig. 5 where operational amplifiers OA_2 and OA_3 in follower configuration were employed for VB_a and VB_c. The CCIIb function is performed by measurement of the output current of OA_1. The measurement was conducted by introducing an impedance in the follower's feedback loop. The negative feedback ensures that the output of OA_1 still follows v_b. The impedance was implemented by the parallel of R_o and C_o so as to also introduce low-pass filtering.

The circuit, besides implementing the proposed topology, was built as an active electrode to experimentally validate the design through in-vivo biosignal acquisition. Therefore, the measured signal was buffered using OA_4 and OA_5 to allow using long lead wires. In particular, the node connected to the inverting input of OA_1 presents no low-impedance paths to ground and is very sensible to coupled currents as occurs with electromagnetic interference coupled to electrode leads [17].

A photograph of the printed circuit board (PCB) is shown in Fig. 6.

B. PROOF-OF-CONCEPT DESIGN RESULTS

In the following subsections, measurements of the parameters obtained with this component selection are displayed and compared to the results of the previous analysis in order to validate it.

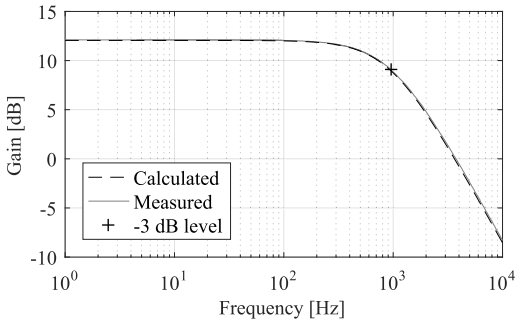

FIGURE 7. Double differential gain of the implemented amplifier.

1) FREQUENCY RESPONSE

The prototype board-level circuit was built as a DC-coupled active electrode, with a DC gain of 4 to improve noise performance by making noise from $OA_{4,5}$ negligible, while retaining an ample DC input range. Impedances were set as resistors with values $R_a = R_b = R_c$ resulting in the following transfer equation

$$v_o = v_{DD}\frac{1}{3R_b}\left(\frac{R_o}{sR_oC_o + 1}\right) \tag{26}$$

where the following factors from (12) can be identified:

$$G_{i,DD} = 1/(3R_b) \tag{27}$$

$$R_T(s) = Z_o(s) = R_o/(sR_oC_o + 1) \tag{28}$$

The transfer characteristic of the circuit was measured using a Stanford SR760 Spectrum Analyzer. Since the analyzer has a differential excitation output, v_a and v_c were short-circuited together and connected to one of its poles while v_b was connected to the other. By the transformation presented in (6) this input translates to an input with a DD component $v_{DD} = 2\ v_i$, hence the analyzer output must be corrected by a factor of 2 to represent G_{DD}. Fig. 7 shows the measured gain together with a transfer obtained by using (26) with the implemented values, where a 12 dB gain and 930 Hz cut-off frequency (marked with a + sign) are shown to have been obtained.

2) OUTPUT NOISE

The total output noise e_o for this circuit can be obtained using the previously developed equations. As $R_a = R_b = R_c$, and considering $e_{OA_1} = e_{OA_2} = e_{OA_3}$, (24) yields

$$i_{n|e_Y} = \frac{2}{3}\frac{e_{OA_1}}{R_b}, \tag{29}$$

$$i_{n|e_R} = \frac{2}{3}\frac{e_{R_b}}{R_b}. \tag{30}$$

The output stage's noise e_{R_T} has contributions from the buffer's voltage noise (with $e_{OA_4} = e_{OA_5}$), the voltage across Z_o produced by current noise from OA_4, and thermal noise

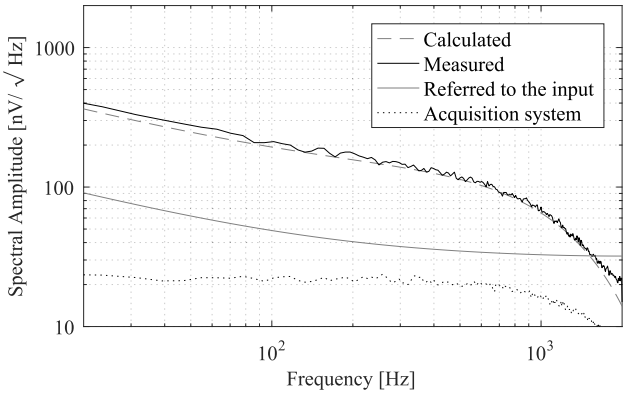

FIGURE 8. Noise spectral density.

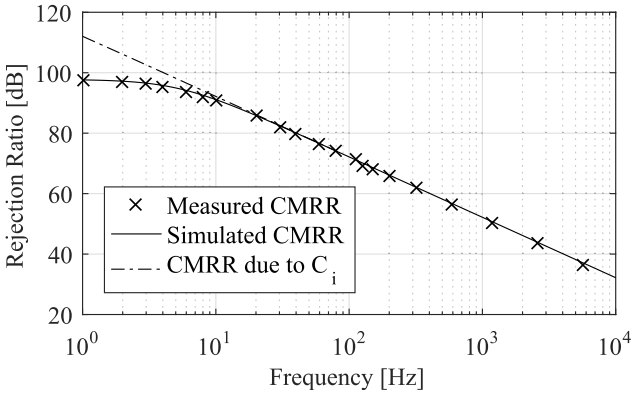

FIGURE 9. CMRR measurement of the implemented amplifier.

from R_o, resulting in:

$$e_{R_T}^2 = \left(\frac{e_{R_o}}{R_o}Z_o\right)^2 + \left(i_{n,OA_4}Z_o\right)^2 + 2e_{OA_4}^2. \tag{31}$$

Therefore, completing (25):

$$e_o^2 = \left(\frac{2}{3}\frac{e_{OA_1}}{R_b}Z_o\right)^2 + \left(\frac{2}{3}\frac{e_{R_b}}{R_b}Z_o\right)^2 + e_{R_T}^2. \tag{32}$$

The noise of the circuit was measured by connecting it to a low-noise differential-input analog-to-digital converter (ADC), ADS1299, configured with a gain of 8 times and 4 kHz data rate. The amplifier inputs were short-circuited to a low-noise 2.5 V reference and the system was placed inside a shielding box connected to ground. Fig. 8 shows a Welch amplitude spectrum estimation of the total noise at the output with a very good match with the noise predicted by (32). In the calculated curve, the ADC's sinc filter response was included. The input-referred noise is also shown, with an integrated noise power in a 10-450 Hz bandwidth of 0.9 μV_{rms}, which is appropriate for biopotential measurements. The acquisition system's noise was simultaneously measured and is shown in Fig. 8 for reference.

3) CMRR

The CMRR was measured using the same equipment at frequencies below 100 Hz and a spectrum analyzer at higher frequencies. G_{CM} was obtained by short-circuiting all inputs to one pole of a function generator and connecting the other to ground. The CMRR was then calculated as G_{DD}/G_{CM} and is shown in Fig. 9.

In this implementation, the CMRR at power-line frequencies was dominated by the input capacitances of the OAs connected to the inverting node of OA_1 (Fig. 5) which produce an analog effect to $G_{mf,b}$ (See Fig. 4 and (17)). A voltage on the equivalent X_b terminal (inverting input from OA_1) appears due to virtual ground and is also applied to the input of OA_5. This node has an impedance $(s(C_{i,OA_1}+C_{i,OA_5}))^{-1}$ drawing a current from the equivalent Z_b terminal, therefore producing a nonzero $G_{mf} = s(C_{i,OA_1} + C_{i,OA_5})$ as per (12). Therefore, from (17), the CMRR is limited by

$$CMRR_{max} = \frac{1}{s(C_{i,OA_1} + C_{i,OA_5})3R_b}. \tag{33}$$

C_{i,OA_1} is 8 pF (common-mode input impedance of TLC2274) and C_{i,OA_5} was measured to be 22.4 pF for TLC2202 (it is not listed in the datasheet). Using these values the calculated CMRR was graphed Fig. 9 showing a good match with the measurement.

At lower frequencies, the CMRR is limited because of imbalances between active components. Applying (19) to this circuit, the equivalent A_{vf} of each OA acting as CCII surrogate has a small departure from unity due to imbalances in their open-loop gain A_{ol} or their CMRR. In buffer configuration

$$A_{vf,OA} \approx \frac{A_{ol}}{1+A_{ol}}\left(1 + \frac{1}{CMRR_{OA}}\right). \tag{34}$$

For example, approximating $A_{ol}/(1 + A_{ol}) \approx 1$ and considering an imbalance $CMRR_{OA_1} = C - \Delta C$ and $CMRR_{OA_2} = CMRR_{OA_3} = C + \Delta C$, (19) yields

$$CMRR_{\Delta} \approx C\left(4\frac{\Delta C}{C}\right)^{-1}. \tag{35}$$

The CMRR of TLC2274 is 75 dB, therefore a 2 % imbalance is sufficient to produce a 97 dB limit for the overall CMRR.

As the CMRR limit given by the OAs' parameter imbalance is higher than that given by the input capacitances of the second stage per (33), the total CMRR can be improved by lowering this capacitance, or by reducing R_b to decrease the time constant in (33) and obtain a CMRR limited only by (35) up to a higher frequency.

The effect of the parasitic impedance Z_n on the CMRR was validated, comparing (15) with measurements soldering capacitors between the sensitive node v_n and ground, and assuming very large R_n values so $CMRR_{v_n} \approx 1/(sR_bC_n)$ at low frequencies. The measurement results are displayed in Fig. 10.

When the "parasitic" capacitance is low enough, the system's CMRR is dominant as seen in the 10 pF line. For higher values, the CMRR starts degrading. The total CMRR results

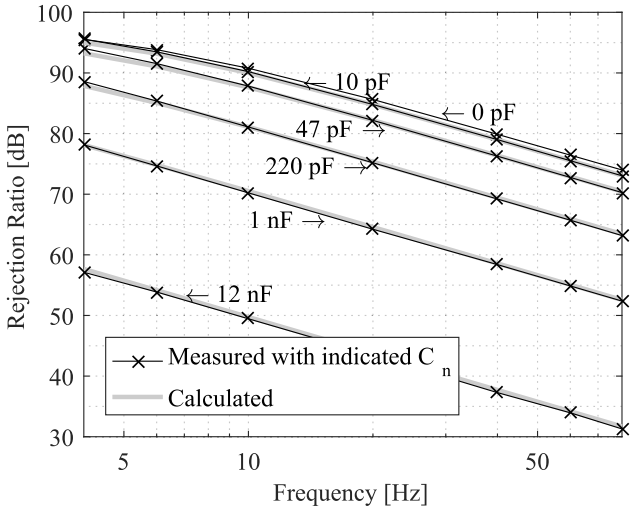

FIGURE 10. CMRR due to parasitic capacitances on node v_n.

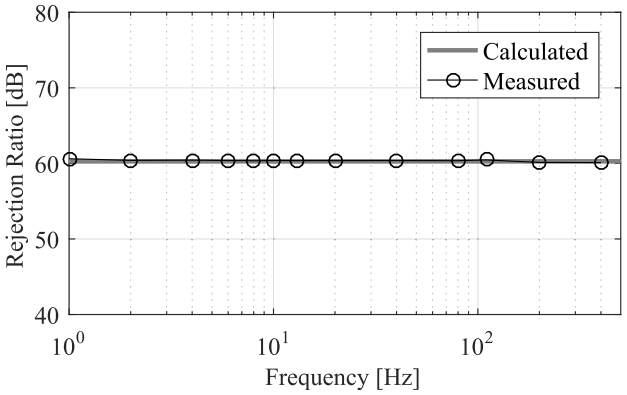

FIGURE 11. Differential mode rejection ratio.

from the combination of the system's CMRR with $C_n = 0$ and that produced by C_n by (15). A lower bound for the total CMRR can be described by compounding these two effects as $(CMRR_\Delta{}^{-1} + CMRR_{C_n}^{-1})^{-1}$ which is graphed in gray line as a reference, closely matching the measurements when the C_n effect is dominant. This result validates (15) as a tool for calculating the highest permissible parasitic impedance for a given set of R_{a-c} and accepted CMRR.

4) DMRR

Finally, R_a and R_c resistors were measured with a $6^{1/2}$ digit multimeter and (22) evaluated to be 60.2 dB. The DMRR was then measured by applying the output of a differential function generator to v_a and v_c, and a low-noise 2.5 V reference to v_b. The DMRR resulted in a constant ratio of mean 60.4 dB in the measured bandwidth as seen in Fig. 11, coinciding with the predicted value. The interfering DM contains EMG crosstalk of the same order of magnitude of the DDM EMG of interest, therefore a DMRR above 40 dB is sufficient.

C. IN-VIVO DD EMG VALIDATION

The amplifier was validated using it for in-vivo tests. It was used as an active electrode for a previously reported acquisition equipment [35], which has 8 differential channels with 24-bit sigma-delta analog-to-digital converters and provides a 5 V supply as well as a 2.5 V reference. The system is connected to a PC through a standard USB bus, and its analog and data conversion stages are galvanically separated from the rest of the acquisition system through an ADUM6401 isolation chip from Analog Devices, which provides both data and power isolation.

The DRL from the equipment was used to set the DC bias of the body, placing it on the waist. The DD electrode was placed on the forearm and hand clenches were executed to pick up the EMG signals from the finger flexor muscles. Measurements were conducted in accordance with ethical guidelines following a research plan approved by La Plata National University bioethics committee. The setup can be seen in Fig. 6b. A sample signal with 3 clenches executed during a 20 s period can be observed in Fig. 12a.

In order to verify the DD function, the output of the DD circuit, v_o, was measured with one channel of the acquisition equipment, and each individual electrode signal was measured with additional channels. For this purpose, the active electrode was fitted with two additional wires carrying the output signal from the two buffers to capture v_a and v_c. The output of OA5 was also recorded in an additional channel to obtain v_b. A benchmark DD signal $\hat{v_o}$ was then obtained digitally by applying (1), and all signals were filtered with a 1 pole Butterworth passband filter between 30 Hz and 450 Hz. The result of the DD signal v_o captured with the DD electrode is marked in black in Fig. 12b, and the calculated DD signal $\hat{v_o}$ in grey. The DC offset between the signals was introduced for visualization purposes. The correlation of the observed 2 s long record of the output of the DD amplifier v_o with the digitally calculated DD signal was 96.5 %, showing that the topology effectively performs the double differential operation in practical EMG measurements.

D. REMARKS AND DISCUSSION

The feasibility of implementing a front-end capable of exact DD EMG measurements with the proposed topology has been demonstrated through a board-level implementation that validates the circuit and the equations obtained through its theoretical analysis.

The features of the proposed topology are displayed in table 1 in comparison with those previously presented in the literature and shown in figure 1.

As expected, the proposed topology can provide a high CMRR limited by the imbalance of the individual CMRRs of its constituent active parts and by the G_{mf} of the CCII. Moreover, the degradation of this CMRR is inversely proportional to the imbalance between the electrodes' impedances, instead of their absolute value as is the case with the 3 IA amplifier of the topology in Fig. 1a.

From the first row of Table 1, it can be seen that the circuit presented in this work has a low active-part count.

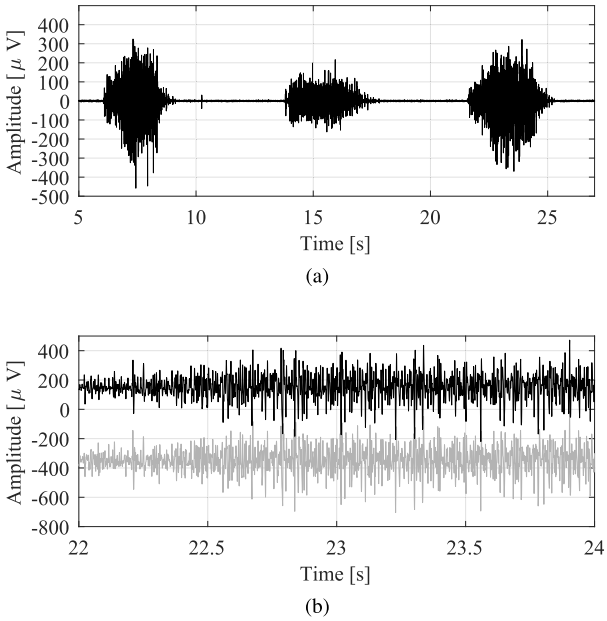

FIGURE 12. Experimental EMG measurements. (a) Measured EMG signal. (b) Comparison of the DD output (dark line) against a digitally obtained DD signal simultaneously acquired using the same electrode locations.

TABLE 1. Parameters of the proposed DD topology vs. previously published DD front-ends.

	Fig 1a	Fig 1b	This work
Active part count	3 IA	4 OA	2 OA , 1 CCII
CMRR*	$C\left(\frac{\Delta C}{C}\right)^{-1}$	$min\,(C, A_{ol})$	$min\left(C\left(\frac{4\Delta C}{C}\right)^{-1}, C_{G_{mf}}\right)$
CMRR due to Z_i, Z_E †	$\frac{Z_i}{Z_E}$	$\frac{Z_i}{\Delta Z_E}$	$\frac{Z_i}{\Delta Z_E}$
Output	SE	Differential	SE

* C: CMRR of active parts. † Z_i input impedance, Z_E electrode impedance, ΔZ_E electrode impedance imbalance.

The proof-of-concept implementation required 2 OAs as voltage buffers, 1 OA instead of a CCII, and the addition of 2 OAs for low-impedance patient-lead connections. However, the buffer OAs are not a necessity for obtaining the DD output (for example considering a use-case as an on-board AFE with an ADC).

The measurements showed a very good agreement between the circuit model, the design equations, and the obtained results. A summary of the resulting parameters characterizing this implementation is presented in the first column of Table 2.

Of course, the performance parameters per se are strongly dependent on the selected commercial components. Therefore, using the criteria stemming from the previous analysis, a second implementation was realized. Indeed, as the CMRR was degraded by the parasitic capacitance of the buffer amplifiers (OA_4 and OA_5) that impacted on the equivalent G_{mf}, an OA with 10 times lower input capacitance was selected (OPA4243, $C_i = 2\,\text{pF}$) and R_b was reduced with the consequence of a more than 20 dB improvement in CMRR at $50Hz$.

TABLE 2. Implementation component list and parameters.

Component selection		
	Selection 1	Selection 2
$OA_{1,2,3}$	TLC2274	OPA4243
$OA_{4,5}$	TLC2202	OPA4243
Z_b	4.3 kΩ	4.7 μF+1 kΩ
$R_{a,c}$	4.3 kΩ	1 kΩ
R_o, C_o	51.6 kΩ, 1.2 nF	300 kΩ, 100 pF
Parameters		
DD Gain	12 dB	40 dB
Bandwidth	0 - 930 Hz	10 - 450 Hz
RTI noise 10-450 Hz	0.9 μV_{rms}	1.4 μV_{rms}
CMRR @ 50 Hz	78 dB	103 dB
DMRR	60 dB	68 dB
DC Input range	±250 mV	Rail-to-Rail
Supply	5.5 mA, 5 V	360 μA, 5 V

Moreover, since OPA4243 is a new generation OA, despite its more expensive cost, also a lower power consumption is obtained. This implementation showcases the versatility of the topology by adding a DC-blocking capacitor C_b in series with R_b to attain an AC-coupled active electrode with a higher amplification and DC input range.

The parameters used in the second implementation are shown in the second column of Table 2. While the previous implementation (Selection 1) was useful for exposing the nonideal factors affecting the circuit's performance and validating the equations, the second implementation (Selection 2) is best suited for comparison with state-of-the art devices, and it shows how an alternative component selection modifies performance in agreement with the analysis conducted in this paper.

Table 3 provides a reference comparison against EMG front-end designs. It is worth noting that although the proof-of-concept implementation was built using off-the-shelve commercial components, it has achieved performance parameters within the state-of-the-art, except, of course, for the power consumption, since carefully designed ASICs can achieve more than an order of magnitude better performance. Although optimizing power consumption falls outside of the scope of this work, the low active-part count compared with other DD front-ends and the power reduction achieved by modifying component selection are preliminary evidence that this feature could be improved in a specialized implementation including ultra-low-power active-block realizations [37], [38].

V. CONCLUSION

A double-differential amplifier topology based on current mode circuits has been proposed. Three type II current conveyors allow implementing an amplifier useful for a DD sEMG electrode, with an optional transimpedance and buffering stage if voltage output is desired. The topology is

TABLE 3. Parameter comparison with EMG readout front-ends.

Key	ISCAS'17 [36]	TBIOCAS'16 [18]	CICC'20 [11]	TCAS-I'20 [10]	This work *
Type †	D EMG/ECG	DD EMG	D EMG/ECG	D EMG	DD EMG
Implementation	ASIC	Discrete	ASIC	ASIC	Discrete
Noise	$1.34\,\mu V_{rms}$ 0.05-11 000 Hz	$1.6\,\mu V_{rms}$ 17-500 Hz	$3.52\,\mu V_{rms}$ 1-150 Hz	$2.4\,\mu V_{rms}$ 40-320 Hz	$1.4\,\mu V_{rms}$ 10-450 Hz
CMRR [dB]	84	86	N/A	112	103
Bandwidth	0.05-11 000 Hz	17-150 Hz	1-150 Hz	40-320 Hz	10-450 Hz
Voltage Gain [dB]	30-40	20	35	43-55	40
Supply	1.8 V 18.2 µA	5 V 220 µA	1.8 V 43.8 µW	2 V 3.15 µA	5 V 360 µA
Input impedance	N/A	2 pF	N/A	N/A	2 pF

* As configured in "selection 2" column in Table 2.
† D: differential, DD: Double Differential.

attractive for microelectronic integration using CCII blocks with a low active-part count suitable for the low power consumption and small footprint needed in wearable applications. A CMRR analysis of the topology was conducted to identify relevant parameters: the CMRR depends on the imbalance between active component parameters and parasitic impedances and can hence achieve a very high value.

The feasibility of the topology was proven by building a board-level prototype implementation with commercial components. Using this prototype, the theoretical model was validated including the effective calculation of the DD signal, prediction of the CMRR degradation due to parasitic impedances, and DMRR degradation due to passive component imbalance. Moreover, superficial DD EMG measurements using dry electrodes were successfully achieved with the proposed topology.

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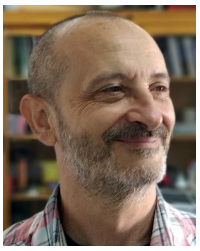

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