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Prologue

This eBook is a compendium of papers presented at the XVIII General Assembly of the Iberoamerican Science and Technology Education Consortium (ISTEC), held in Porto Alegre, Brazil, May 16-20, 2011. Hosted by Pontifícia Universidade do Río Grande do Sul (PUCRS), representatives from various universities in Latin America presented papers in the subjects of library science, cutting-edge technologies, and education.

This Compendium is fully aligned with ISTEC's four Initiatives: (1) Liblink (Library Linkages) network; (2) R&D (Research and Development); (3) ACE (Advanced Continuing Education); and (4) Los Libertadores Centers of Excellence, promoting entrepreneurship and innovation/creativity in engineering education. The thematic areas covered by these works are rich and varied, ranging from cartographic collections, digital repositories and harvesting in libraries, to experimental platforms in digital control technologies, to practical approaches and the role of complexity science in engineering education.

We hope that our readers will enjoy these works, all excellent contributions to the ISTEC vision of life-long learning and team-based approaches to knowledge creation. We also want to extend our appreciation to the Universidad Nacional de La Plata (UNLP), Argentina, host of the ISTEC Liblink Initiative, for undertaking the project of publishing this eBook.

Dulce M. García
President, ISTEC

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Experimental Platform in Digital Control of DC-DC Converters

Santiago Brum, Alejandro De Camilli, Damián Lancieri, Ing. Gabriel Eirea

PEC(DC)[3] – Final Careers Project 2010, IIE – Engineering Faculty – Republic University

Abstract *— This article describes the implementation of a platform for experimentation in Digital Control of DC/DC Converters. This platform will allow us to discuss different techniques for power converters control, assess the state of the art and propose new techniques for specific applications in chip development or electronic systems. The platform consists of a DC/DC Buck type converter, two variable resistors, four A/D converters and a PID controller developed in an FPGA. The modular design allows us to add different converters, fillers and methods of control.*

Keywords: A/D Converter, Analog-digital conversion, Buck Converter, DC/DC Converter, DC-DC power converters, Digital control, Dynamic load, FPGA, Switching converters.

I. INTRODUCTION

This article describes the construction of an experimental hardware platform, consisting of power converter modules and a digital controller module.

The power modules (DC-DC regulators, AC-DC rectifiers and DC-AC inverters) cover a range of low, medium and high power applications and have already produced some successful commercial products [1,2,3]

The purpose of this project is to consolidate a working group to develop techniques for modeling and to allow the control of switched circuits, especially in power electronics applications for effective and efficient conversion of electrical energy.

This work is part of a CSIC[1] project of research and development to consolidate the control group of power electronic converters. The power modules (DC-DC Regulators) cover a wide range of applications of low and medium power, particularly for voltage regulation in portable electronic systems and computer equipment. The controller module is based on an FPGA with a PC programming interface.

II. FUNCIONAL SPECIFICATION

The system consists of a digital control module implemented with an FPGA[2] on the card IIE-Cyclone-II[3] [4, 5] and three types of peripherals: Resistive Dynamic Load, A/D Converters and two DC/DC converters, one Buck single phase converter and one Buck multiphase converter.

The control module and peripherals are the experimental platform of digital DC/DC control converters.

The FPGA will be responsible for performing the digital control of DC/DC converters and for analyzing the data from the output voltage and current of DC/DC converters that come through the A/D converter, while controlling the output voltage. Another task of the FPGA is to determine the dynamic load value commanded from the PC.

The single phase converter converts 5V to 3.3V and works up to 10A of current. The multiphase converter, converts from 12V to 1,5V up to a maximum current of 50A.

The A/D converter reads the tension or the current of the converter and sends the correct digital word to the FPGA.

The Dynamic resistive load receives a binary word from the FPGA and generates a combination of resistances. It is responsible for control of the dynamic demand for power to the DC/DC converters.

[1] In Spanish: Comisión Sectorial de Investigación Científica, UdelaR

[2] Field Programmable Gate Array

[3] It is the final product of another IIE project based in a Cyclone-II card of ALTERA [5,10]

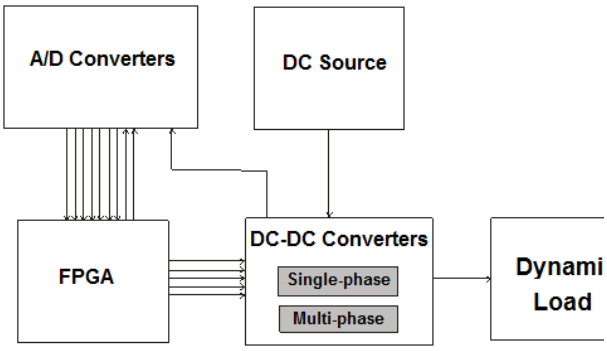

Figure 1. Dynamic load block diagram

III. DESIGN

A. Resistive Dynamic Load

In order to test the DC/DC converters, resistor values between 0.016Ω and 50Ω are needed. However, there are plans to work in two more DC/DC convertors, so another range of loads between 50Ω and 40KΩ was considered.

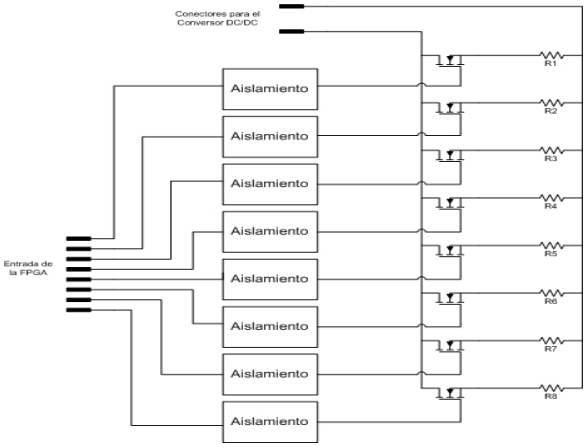

Figure 2. Dynamic resistive load scheme

There are only 8 bits of the FPGA available for changing the load, so some values were chosen to work in the adequate range.

TABLE I
FIRST RANGE OF LOAD VALUES

Word	Value (Ω)
00000001	0.02
00000010	0.33
00000100	1.50
00001000	4.00
00010000	10.00
00100000	20.00
01000000	40.20
10000000	50.00

TABLE 2
SECOND RANGE OF LOAD VALUES

Word	Value (Ω)
00000001	50
00000010	100
00000100	500
00001000	1000
00010000	8200
00100000	13000
01000000	30000
10000000	40200

In Figure 3, a schematic of how to perform the control of the MOSFETs transistors with the FPGA, which delivers a voltage of 3.3V, is shown. This voltage passes through an optocoupler to isolate the FPGA from the rest of the circuit, then a driver to adapt the signal to the MOSFET.

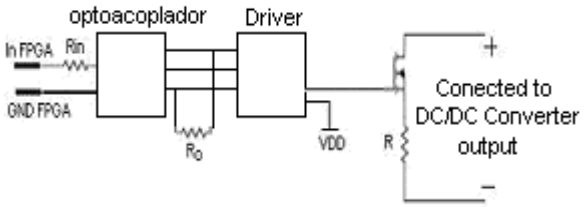

Figure 3. Load branch scheme

Rin resistance works both by limiting the current that is required for the FPGA and by supplying enough current to power the diode.

As a means for testing the loads, the pins for the FPGA were connected, binary words from the PC were entered, and the value of output resistance was checked. The results are shown in Table 3 and 4.

TABLE 3
FIRST RANGE OF LOAD EXPERIMENTAL VALUES

Word	Theoretical Value (Ω)	Measure Value (Ω)
10000000	0.030	0.4
01000000	0.33333333	0.53
00100000	1.5	1.7
00010000	5	5.18
00001000	10	10.29
00000100	20	20.32
00000010	40	40.45
00000001	49.9	49.96

TABLE 4
SECOND RANGE OF LOAD EXPERIMENTAL VALUES

Word	Theoretical Value (Ω)	Measure Value (Ω)
10000000	49.9	49.8
01000000	100	99.8
00100000	560	559
00010000	1000	998
00001000	8200	8140
00000100	13000	12970
00000010	30000	29900
00000001	40200	40000

B. A/D converter

Figure 4 shows the stage of the signal and the A/D converter conditioning in a block diagram. Adaptation of the signal of interest from the DC/DC converter to the range of values that the A/D converter can handle will occur during this stage.

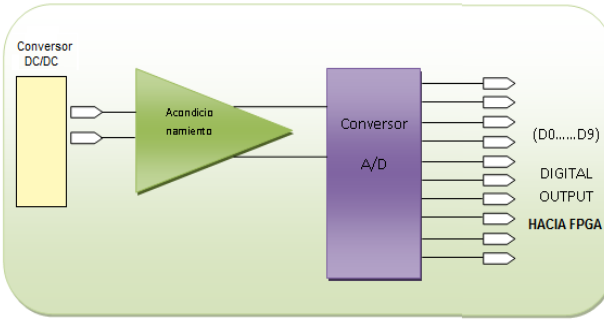

Figure 4. A/D converter block diagram

As a first step a boost or reduction of the input voltage was implemented, being necessary to encompass the whole range of the converter. In a second step the signal is filtered by a low pass filter (LPF Low Pass Filter) with a cutoff frequency (fc) less than half the sampling frequency (fs) of the converter, to eliminate the aliasing effect. Figure 5 shows a block diagram of the conditioning step.

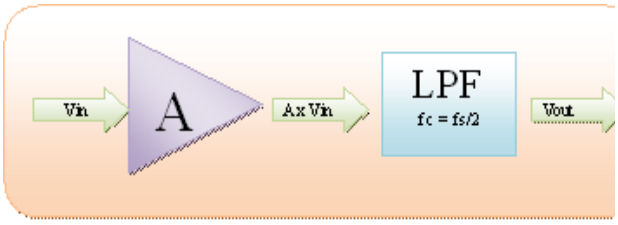

Figure 5. Conditioning step diagram

Conditioning requires different types of boost or reduction, which were implemented by means of mechanical jumpers.

TABLE 5
A/D CONVERTER AMPLIFICATION GAINS

Vi	Gain	Vo
1	1	1
1.5	2/3	1
10	1/10	1
20	1/20	1

Signal filtering is performed using an active filter of first order with cutoff frequency at 1MHz. It is shown in the diagram in Figure 6.

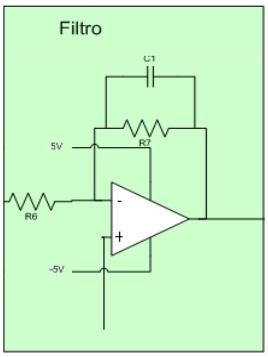

Figure 6. Anti-aliasing filter

In order to get a good resolution, a 10 bit Texas Instruments ADS822E converter was chosen, with 40MSPS sampling rate and a latency of less than 0.5 us.

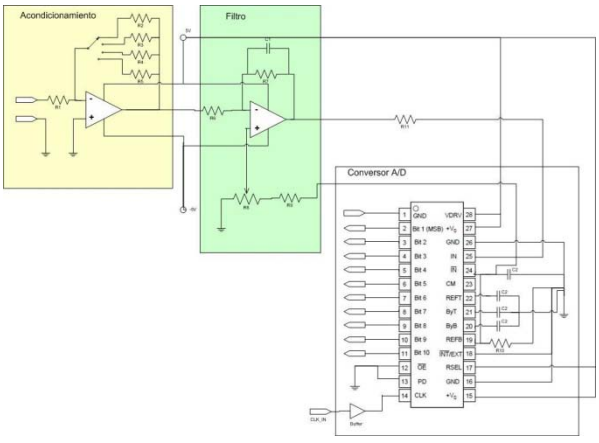

Figure 7. Common mode A/D converter diagram

Figure 7 shows a converter diagram with

common mode input. This converter allows us to measure the DC/DC converter output with greater precision.

Figure 8 shows a diagram of a differential input converter, its configuration allows measuring voltage or current values of any component since it can take negative values.

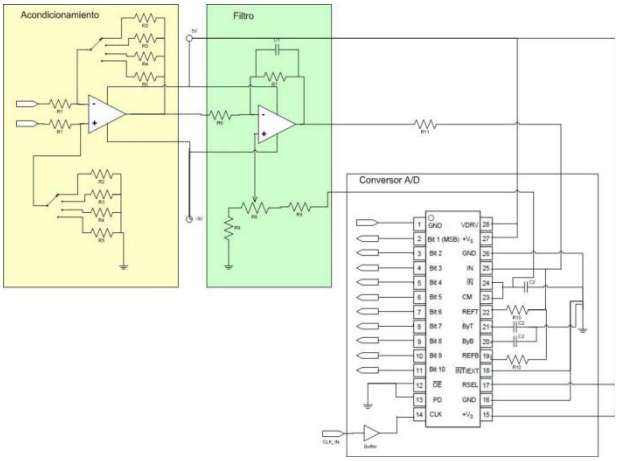

Figure 8. Differential input A/D converter diagram

Test results are shown in Figures 9 and 10. They are average values obtained by the FPGA.

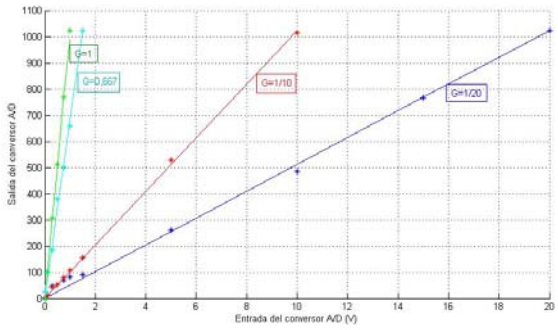

Figure 9. Test input common-mode converter.

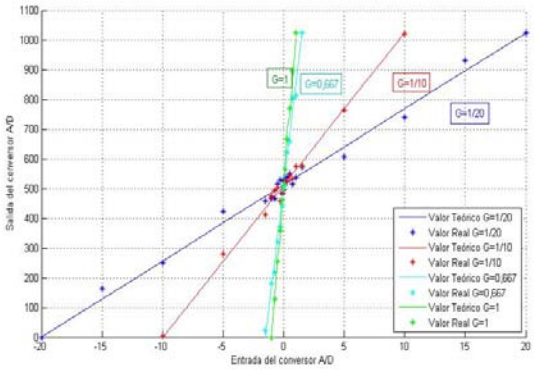

Figure 10. Test input differential-mode converter.

C. DC-DC Converters

Converter Buck single-phase

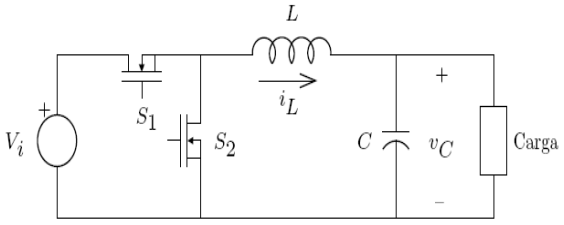

Figure 11. Single-phase DC/DC Converter Scheme [7]

In Figure 11 a basic diagram of the single-phase Buck converter is shown. To calculate the components values, three principles of the system in regime were taken into account:

1) *Volt • Second Balance: the average value of the applied voltage on an inductor must be zero.*
2) *Load balancing: the average value of the current through a capacitor must be zero.*
3) *Small ripple assumption; we can approximate the voltages on the capacitors at their DC values, and in some cases, approximate the currents by inducing their DC values (though for instance, this is not true in DCM). [7]*

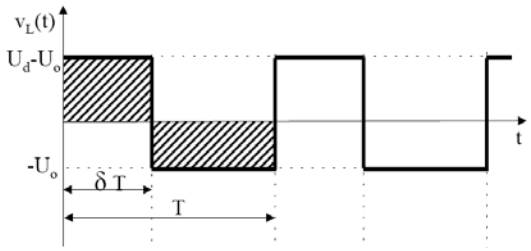

Figure 12. Voltage applied to the inductance. [6]

In Figure 12 the voltage applied to the inductance of the filter is shown. Applying the first hypothesis the average voltage on the inductor is taken as zero:

$$\langle v_L \rangle = \frac{1}{T}\int_0^T v_L(t)dt$$

$$= \frac{1}{T}\left[(U_d - U_o)\delta T - U_O(1-\delta)T\right]$$

$$U_d\delta - U_O = 0 \Rightarrow \frac{U_o}{U_d} = \delta \quad (1)$$

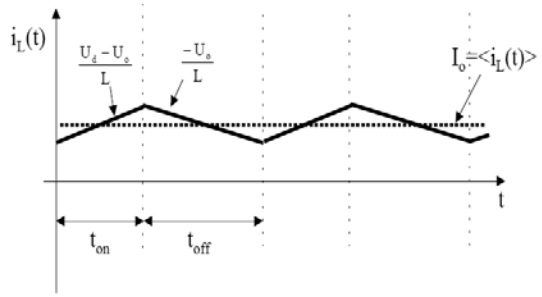

Figure 13. Current through the inductor

Figure 13 shows the current in the inductance. Equation (2) can be derived.

$$\Delta I = \frac{U_d - U_o}{L}\delta T \text{ , and being } \frac{U_o}{U_d} = \delta$$

$$\text{then } \Delta I = \frac{U_d T}{L}\delta(1-\delta) \quad (2)$$

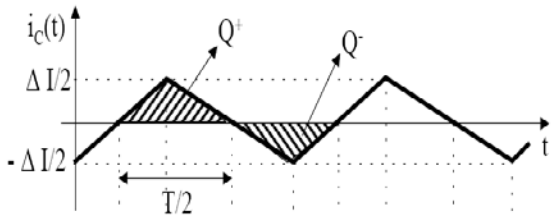

Figure 14. Current through capacitor [6]

In Figure 14, ΔI represents the ripple current from the capacitor (and therefore inductance) and Q+ and Q-, the maximum and minimum loads, respectively, which the capacitor will have.

To calculate the output ripple voltage of the converter, the maximum accumulated charge on the capacitor Q+ is to be considered. Then in Figure 14 we have:

$$v_C(t) - v_C(t_0) = \frac{1}{C}\int_{t_0}^{t} i_C(t)dt$$

$$\Delta v_C = \frac{1}{C}\frac{1}{2}\frac{T}{2}\frac{\Delta I}{2}$$

Substituting in equation (2):

$$\Delta v_C = \frac{T^2}{8C}\frac{U_O}{L}(1-\delta) \quad (3)$$

Defining: $\omega_C = \frac{1}{\sqrt{LC}} = 2\pi f_C$ and $f = \frac{1}{T}$ the following expression is obtained for the relative output voltage ripple:

$$\frac{\Delta v_C}{U_o} = \frac{\pi^2}{2}(1-\delta)\left(\frac{f_C}{f}\right)^2 \quad (4)$$

Considering the real capacitor model as an ideal capacitor in series with a resistance and if it is significant, the output voltage ripple can be approximated by $\Delta v_C = V_{ESR} = RI_o$

For the converter design, the output voltage ripple was considered to be less than 5%, the ripple of the current must be less than 30% of the maximum current Io, and work will be performed with a value of T = 1.28ms.

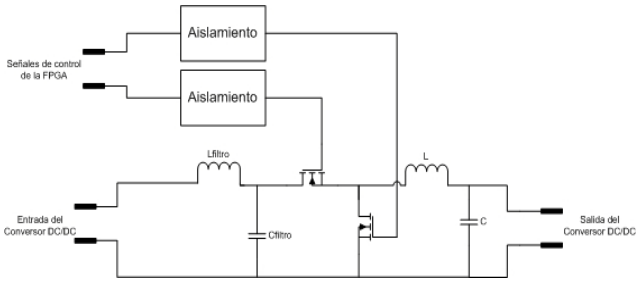

Figure 15. Single phase converter diagram

The single-phase converter converts 5V to 3.3 V and using equation (1) the following was obtained:

$$\Delta v_C \le 0{,}1\ 6V5 \text{ y } \quad \delta = \frac{U_o}{U_d} = \frac{3{,}3V}{5V} = 0{,}66$$

Substituting these values in the equation (4) and working out LC, it can be found that:

$$L\ C \ge 1{,}4 \times 1\ 0^{1\ 2} \quad (5)$$

The converter was designed for a range of 0.1 A to 10 A, then the ripple current status is $\Delta I \le 3\text{A}$. If this value is substituted in equation (2) the second inequality is found:

$$L \ge 0{,}4\ 8\ \mu H \quad (6)$$

From (6) y and (7) L = 0.5 μH y C=3 μH were chosen.

A filter consisting of an inductor and a parallel capacitor was placed in the input of the converter, this filter serving to isolate the equipment connected to the input from the noise

introduced by the switches.

Buck multiphase converter

The multiphase converter designed converts 12 V to 1.5 V, being similar to the single-phase one but with four inductors instead of one, switches being activated in out of phase by a quarter period, discarding the first order current harmonics and getting a smaller ripple.

As in the single phase converter, it can be calculated that:

$$\delta = \frac{U_o}{U_d} = \frac{1{,}5V}{12V} = 0{,}125$$

The current ripple for each branch of the converter must be less than 30% of the maximum current for each branch and a period of 1.28 microseconds was used.

As the converter was designed for a maximum load of 50 A and a 4-phase converter was desired, the condition of the ripple current in each branch is:

$$\Delta I = \frac{U_o T}{L}(1-\delta) \le \frac{50A}{4} \times \frac{30}{100} = 3{,}75\ A$$

The condition to be met by the inductance of each branch of the converter is:

$$L \ge 0{,}4\ 4\ \mu H$$

To determine the capacitor value it is necessary to take into account that the output voltage ripple should be less than 5%, as in the case of single-phase converters.

$$v_C(t) - v_C(t_0) = \frac{1}{C}\int_{t_0}^{t} i_C(t)dt$$

$$\Delta v_C = \frac{1}{C}\frac{1}{2}\frac{T}{2}\frac{\Delta I_T}{2}$$

Being iC(t) and ΔI_T the current and the total current ripple through the condenser respectively. Therefore, in order to determine the value of C the only additional data needed is ΔI_T .

The current iC (t) is the sum of the currents through the four branches of the converter which are like those in Figure 14 but with offsets of 90° between them. While finding the sum, a periodic triangular wave is obtained. Figure 16 shows how the slopes of each leg of the triangle wave - that results when the original function f (t) have slope "a" in (0. δT) and "b" in (δT.T) for the four possible cases: 0<δ<0.25; 0.25<δ<0.5; 0.5<δ<0.75 and 0.75<δ<1 - are.

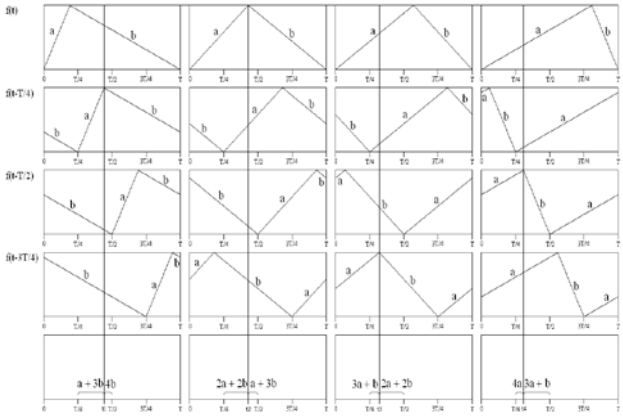

Figure 16. Currents through the branches of the multiphase converter

.

The resulting wave frequency is four times bigger, so the period is 0.32 microseconds.

As in the case of the single phase converter, the duty cycle is 0.125.The case of the first column from the left of the figure above is studied, to analyze the total current.

Having chosen an inductance value of 0.51µHy, the ripple voltage in each branch is 3.29A. Therefore:

$$a = \frac{\Delta I}{\delta T} = \frac{3{,}2\ A\ 9}{0{,}1\ \times 1{,}2\ \mu s\ 5\ 8} = 2\ ,5\ A\ 1\ /\ 6\ s$$

and

$$b = -\frac{\Delta I}{(1-\delta)T} = \frac{3{,}2\ A\ 9}{0{,}8\ \times 1{,}2\ \mu s\ 5\ 8} = -2{,}9\ A/\mu 3$$

By means of these values the total current ripple is calculated as:

$$\Delta I_T = (a+3b)\left(t_1 - \frac{T}{4}\right) = (a+3b)\delta T$$

$$= 1\ ,7\ A/\mu s \times 0{,}1\ \times 1{,}2\ \mu s\ 5\ 8\ 1{,}8\ A\ 8$$

We can obtain C from the ripple voltage equation:

$$\Delta v_C = \frac{1}{C}\frac{1}{2}\frac{T}{2}\frac{\Delta I_T}{2}$$

Recalling the assumption that the output voltage ripple should be less than 5% we obtain that $C \geq 1{,}004\mu F$

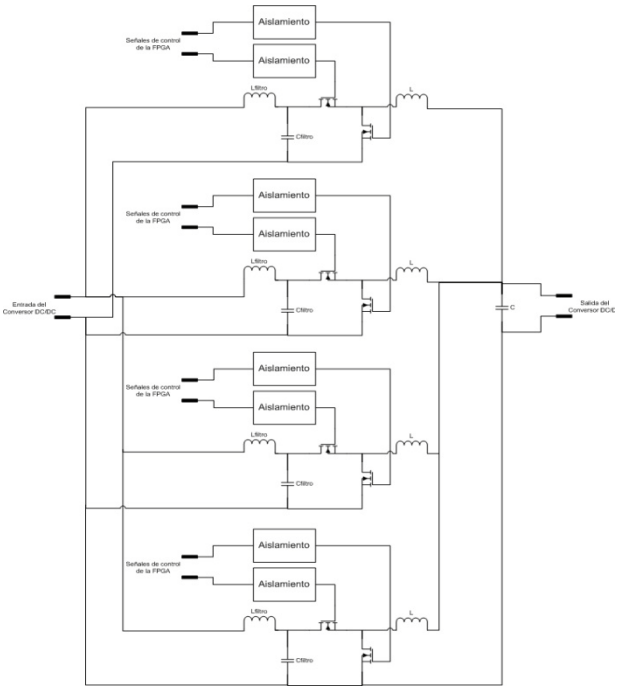

Figure 17. Multiphase converter scheme

D. PWM signal generation for command DC-DC converters

Implementation was performed in VHDL modules that were recorded in the IIE-Cyclone II card allowing the following:

1. Management of Dynamic Loads switch
2. PWM signal generation for the management of the DC/DC converter switches in open loop
3. Feedback output voltage DC/DC converters for closed loop test
4. Generation of clock signal for the A/D converter and the PID controller

In order to create the modules, a modulator implemented as a final project for the subject named Logical Design 2 was used as a reference [9].

The open loop system of the DC/DC converter takes the duty cycle of PWM signals that command the switches (represented by 10 bits) as inputs, and the voltage delivered by the converter as outputs (see Figure 18).

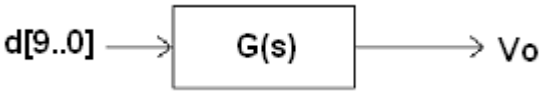

Figure 18. Open loop system

The system shall generate periodic waveforms with the duty cycle d[9..0] and shifted 90º, 180º and 270º between the different branches of the 4-phase converter as shown in Figure 19.

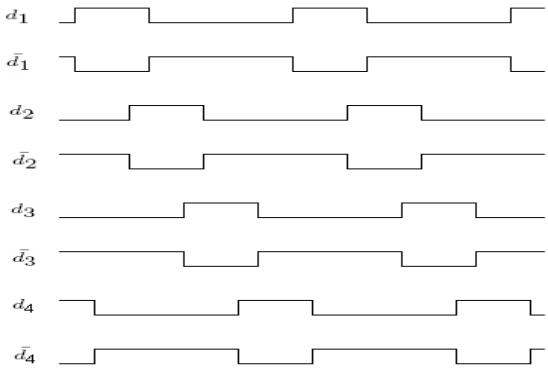

Figure 19. PWM pulses for keys management of a DC-DC multiphase converter.

The following section describes the implementation of a module from a previous work [9] that consists of a pulse width modulator with 10 bits to represent the duty cycle, as shown in Figure 20.

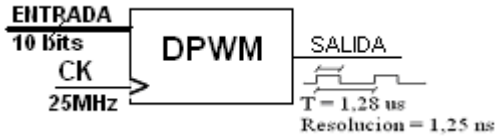

Figure 20. 10 bits Pulse width modulator

This modulator is based on the use of the 8 most significant bits of duty cycle in order to obtain a periodic wave but with 5 ns resolution. We used a counter with the output connected to a comparator, thus producing periodic wave "thickness adjustment".

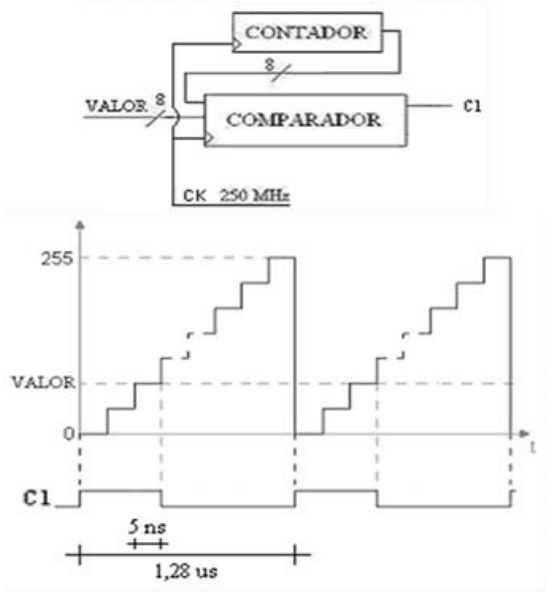

Figure 21. Thickness adjustment

For a resolution of 1.25 ns ("fine adjustment") the 2 less significant bits of duty cycle and a serializer were used.

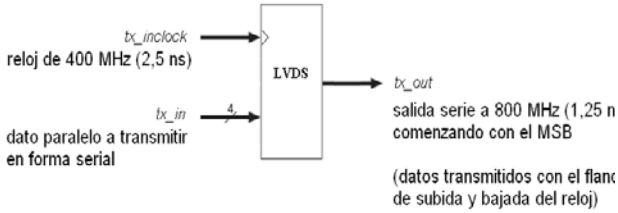

Figure 22. Serializer for fine adjustment

From the thickness adjustment wave and the 2 least significant bits, we can determine which bit and when to put it into the serializer in order to get a resolution of 1.25 ns.

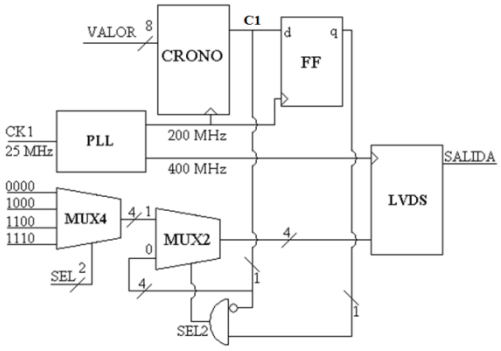

Figure 23. Modulator diagram ([9]).

DPWM

This block is based on the modulator described above and can also generate periodic "Inverse" waves and 90º, 180º and shifted 270º to handle all the switches of a 4 phase DC/DC converter.

The "inverse" waves are the theoretical duty cycle 1-d, where d is the duty cycle that determines the transformation ratio. In this case an additional parameter of 8 bits, SEPARATION, was introduced, which adjusts the inverted wave as shown in Figure 24.

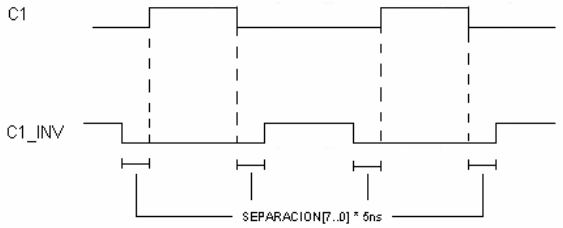

Figure 24. SEPARATION Parameter [7.0]

In Figure 24, C1 represents the periodic wave of thickness adjustment. With this parameter, the length of time that both switches are open simultaneously can be controlled. COMPARATOR INVERSOR block was implemented taking into account the parameter SEPARATION (8). Thus C1_INV gets a resolution of 5 ns.

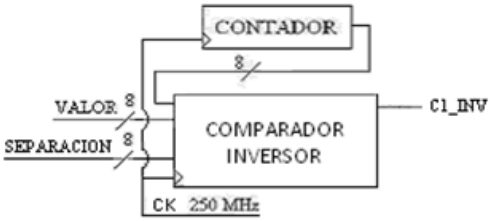

Figure 25. Blocks for generating of "inverse" waves

In order to obtain the shifted periodic waves, the block in Figure 26 was implemented.

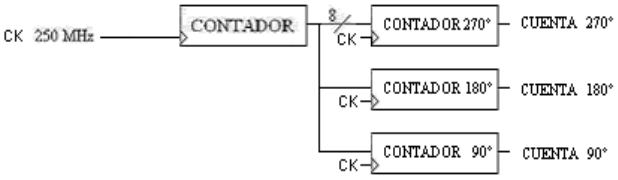

Figure 26. Blocks for generating shifted waves.

Shifted waves 90°, 180° and 270° with respect to a reference were obtained. With each of the counters, wave thickness adjustments were generated. Then higher resolution waves were generated as described above, obtaining

shifted waves with a resolution of 1.25 ns.

E. Control in FPGA implementation

The block for the feedback output voltage DC/DC converter is shown in Figure 27.

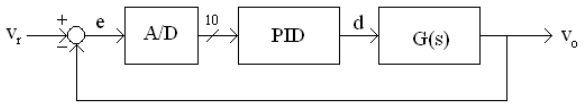

Figure 27. Output voltage feedback

Auxiliary signals were generated and a block for a PID control of the plant was done.

Recycled DPWM

This block is basically the DC/DC system described above with the addition of the following outputs, and a PID block (Figure 27):

CLK_ADC: clock signal period of 640 ns (a half of the PWM period). It is used in the A/D converter and the PID.

CE_PID: Signal for enabling PID block result readings. It is always high, so it only includes the rising edge of CLK_ADC that is half the PWM cycle.

CK_DPWM: clock signal with a period that equals the PWM signal (1.28 us) period but with the rising edge 160 ns before the end of the previous. It is used to load the reading of the DPWM block in the PID controller at the end of the PWM cycle, so as to avoid further changes at the logic level in the PWM signals in the same period.

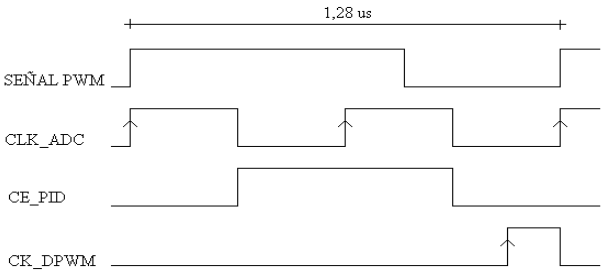

Figure 28. *Auxiliary signals for closed loop control.*

PID

The PID corresponds to the proportional-integral-derivative control of the output voltage of the converters in discrete time. Its entries CLK_ADC, KP, KI, KD and ERROR[9..0] correspond to the output of A/D converter. The output D[9..0] is of the form: D[n] = KP*ERROR[n] + KI*(S[n-1] + ERROR[n]) + KD*(ERROR[n]-ERROR[n-1]), where S[n-1] + ERROR[n] = S[n] is the cumulative sum of the integral term and all the variables that are represented in two's complement.

In order to obtain S[n-1] and ERROR [n-1] (sampled values earlier than n) type D flip-flops with clock CLK_ADC were used (see following figures).

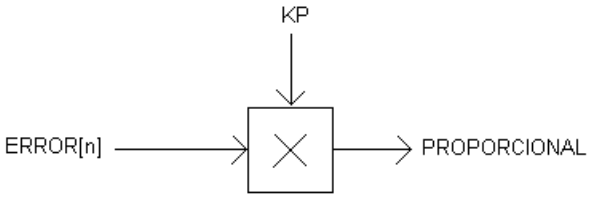

Figure 29. Proportional block diagram

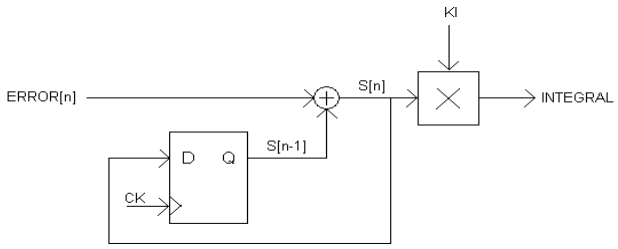

Figure 30. Integral block diagram

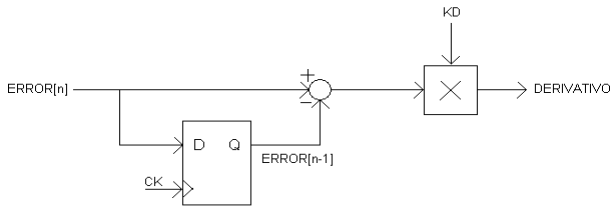

Figure 31. Derivative block diagram

To perform the multiplication and sum of the vectors of the relationship that defines D[n], configurable blocks existing in the Cyclone II chip are used.

The block that calculates the integral term is designed so that S[n] saturates at -2048 and in 2047.

For simplicity purposes, the detailed

calculation of the controller constants is not shown, the constants obtained being:

KP = 0.12628 KI = 0.06186 KD = 0.02596

As work is done on the binary system, it is approximated by:

KP = 0.001000 KI = 0.000011111 KD = 0.0000011010.

It was decided to work with constants of 6-bit with their format:
<1 bit of sign><2 bits>,<3 bits> for performing the operations in the controller with a fixed number of bits regardless of the values.

Therefore, for the above values, a shift of the dot of 1, 6 and 6 places to the right for KP, KI and KD was applied respectively, then obtaining the following constants in the format explained above:

KP = 000.010 KI = 011.111 KD = 001.101.

With this format for the constants and taking into account that ERROR is 10 bits and S (sum of the integral term) is 12 bits, the proportional term gets the form: <13 bits>,<3bits>; the integral <15 bits>,<3bits> and the derivative <13 bits>,<3bits>.

Now, we must undo the shift of the dot applied to the constants. So the format of the proportional term is: <12 bits>,<4 bits>; the integral <9 bits>,<9 bits> and the derivative <7 bits>,<9 bits>.

To make the sum of the three terms, they must be in the same format: <12 bits>,<9 bits>.

Therefore it may be necessary to extend the decimal bits by adding zeros to complete 9-bit and make a sign extension to complete the entire 12 bits (repeating the sign bit as many times as necessary to be a two's complement).

The result of the sum is obtained in the form: <14 bits>, <9 bits> (there are 2 additional bits for the case of carry). D (duty cycle) is obtained from the fractional part of the sum, taking into consideration:

1. If the integer part is > = 1, then D = 1111111111 (1023)
2. If the integer is negative, then D = 0000000000 (0)
3. Otherwise, D is the fractional part of the sum by adding a zero to make 10-bit LSB

IV. PLATFORM TESTS

The following tests were performed: response to the variation of duty cycle, response to load variation, and transient test.

In this article, only the test of the single-phase DC/DC converter is presented, having postponed the multi-phase test for a second stage.

The test of the response to the duty cycle variation consists in taking samples of the voltage of the converter output, with constant input voltage and load. We did the test with an input voltage of 5V and a load of 1kΩ.

The duty cycle is changed from 0.1 to 0.9 taking 11 samples of the output voltage. In Figure 32 the output voltage obtained is plotted as a function of duty cycle, and it can be noticed that the graph is monotonic and pretty close to the ideal line.

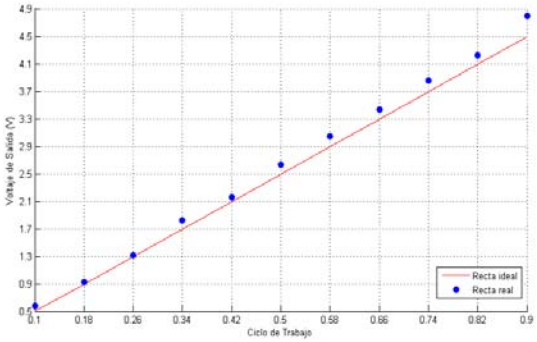

Figure 32. Output voltage of the single-phase converter vs. a variation of duty cycle

The test of the load variation response consists in taking samples of the converter output voltage during a variation of the load demand. At the beginning, there was a high level of noise in the gate. This problem was almost eliminated by removing the gate capacitors and adding one 22nF capacitor connecting the common point to the two MOSFET and to the circuit ground. For this new configuration, the converter output voltage

with a duty cycle of 0.66 was 3.66 V

We connected the load to the single-phase converter, and through the FPGA we gradually altered the values of the load; the results are shown in Table 16. In the graph of Figure 33 we can see the voltage evolution vs. the current.

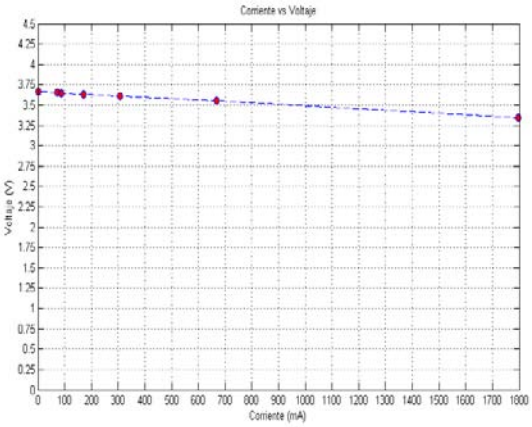

Figure 33. Response to load variation: Voltage vs. current.

The transient test in open-loop transient consists in triggering a drop in the load (an increase in current consumption) and taking samples of the induced change in the output voltage of the converter. For this, as with the previous test, the converter and the load are connected and the oscilloscope is set to perform a single shot.

The test was conducted with a duty cycle of 0.66, and an input voltage of 4.97 V, the drop was made from the burden of 49.96 Ω to 1.7 Ω. In Figure 47 it can be noticed that in the response to this step, the transition takes 29.2 ns and the change is from 3.66 V to 3.35 V through a minimum voltage of 1.94 V.

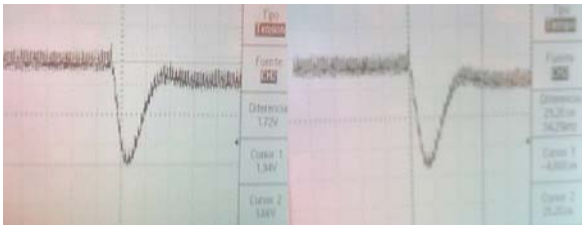

Figure 34. Response to a Load drop

The final circuit is shown in Figure 35, its main components and the input and output values being marked. The energy flows from right to left through the series inductance Lf and capacitor Cf in parallel to form the input filter, then come the high MOSFET in series and the low MOSFET in parallel, then the main components of the converter which are the inductor Lc in series and parallel capacitor Cc.

The converter control is performed by the FPGA through the IN Low which controls the MOSFET handling the low MOSFET and the input IN High which handles the high-MOSFET.

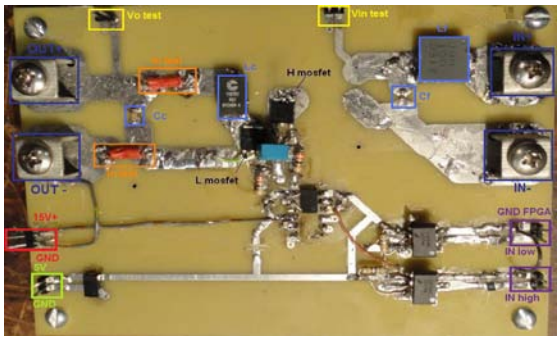

Figure 35. Final circuit of the Multiphase converter

Finally we tested the single-phase converter with the variable load, the A/D converter and the FPGA. With this system, we changed the load through the computer and the FPGA reacts maintaining the output voltage stable.

In the bottom of Figure 37 we can see the feedbacked converter output voltage and the upper part of the figure is the high MOSFET input, we can notice that the controller saturates and goes from 0V to 5V. In Figure 36 we can see the two entries where we can observe that while a switch period is open (3.3 V low active), the other opens and closes. We can also see that the controller reacts to the input signal A/D converter.

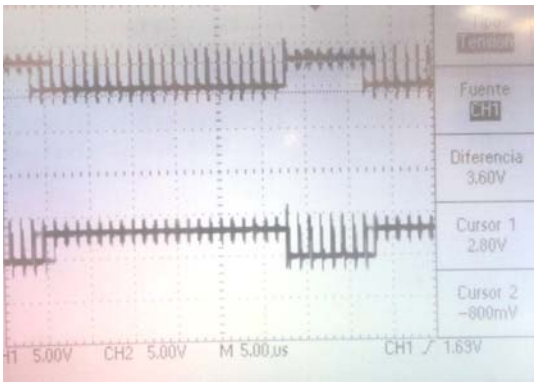

Figure 36. FPGA output with the first constants

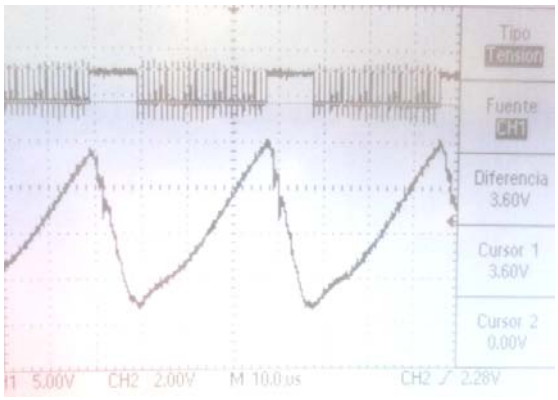

Figure 37. Voltage output of the converter with the first constants of the FPGA.

In order to improve this response, PID gain was changed until a stable output was obtained. Nevertheless, the 3.3 uF output capacitor was increased by means of putting a 10uF capacitor in parallel, in order to better stabilize the output. In this way the voltage was stabilized at 3.6V.

In Figure 38, the PWM outputs of the FPGA are shown. The switches are activated by low voltage.

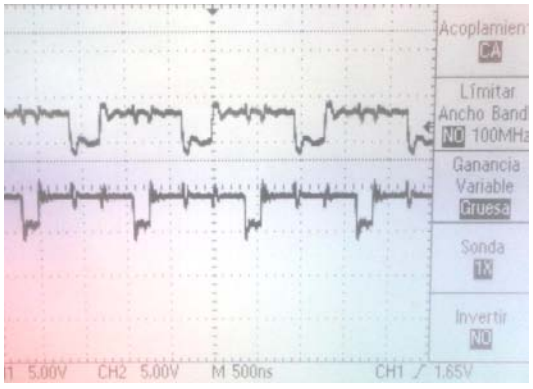

Figure 38. FPGA output with the new constants.

Figure 39 shows the output voltage ripple when the converter is without load and in closed loop. The ripple is 146mV peak to peak which represents a 4.4% of the output voltage.

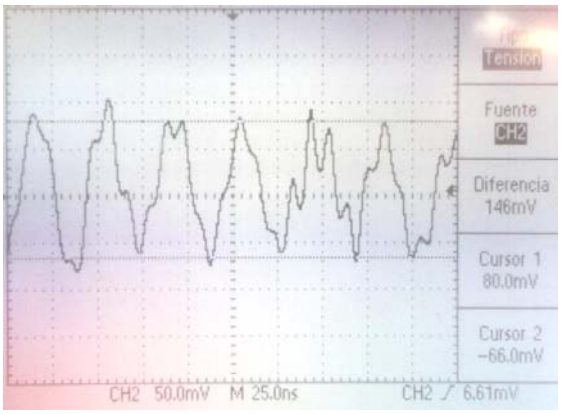

Figure 39. Output voltage ripple of the converter.

V. CONCLUSIONS

Once the project was completed, the single-phase Buck converter and the four A/D converters were put into operation, the dynamic load circuits for two different ranges were ready to use, and the PID control loop was implemented. This loop needs some adjustments in the constants of the control blocks (proportional, derivative and integral) for maintaining the output voltage constant while DC/DC current demand is altered. The platform was tested with the single-phase Buck converter both in closed loop and in open loop, and new algorithms can be tested on it.

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Digital Library of Historical Cartography

Open access to cultural heritage and public good

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Abstract *— This paper describes the integration of information between the Digital Library of Historical Cartography and the Bibliographical Database (DEDALUS), both of the University of São Paulo (USP), to guarantee open, public access via Internet to the maps in the collection, making them available to users everywhere. This digital library was designed by the Historical Cartography Studies Laboratory team (LECH/USP), and it provides map images on the Web, of high resolution, and presents the information on these maps as technical-scientific data (projection, scale, coordinates). It also offers printing techniques and material support that have made their circulation and cultural consumption possible. The Digital Library of Historical Cartography is accessible not only to the historical cartography researchers, but also to students and the general public. Beyond being a source of information about maps, the Digital Library of Historical Cartography seeks to be interactive, exchanging information and seeking dialogue with different branches of knowledge.*

Keywords*:* Cartographic collection, Databases (keywords), Digital libraries, Historical cartography.

I. INTRODUCTION

The Digital Library of Historical Cartography [1] makes high resolution digital reproductions of maps printed between the 16th and 19th centuries that belong~~ing~~ to the University of São Paulo (Brazil) collections available. Each map is presented with carto-bibliographical and biographical references, and relevant technical, editorial and historical information for the analysis of the cartographic documents.

The group of digital libraries of the University of São Paulo (USP) contains the Brasiliana USP [2], the Digital Library of Rare Books [3] and the Digital Library of Theses and Dissertations [4]. The Digital Library of Historical Cartography consists of a collection of digitized copies of the printed maps of the former Santos Bank, about 250 in number, which are currently in the custody of the Institute of Brazilian Studies, University of São Paulo (IEB/USP), as determined by the Brazilian Federal Court. The IEB is responsible for the digitalization of maps and also for the conservation of the originals [5].

The Digital Library of Historical Cartography seeks to be a dynamic repository of information (technical and carto-bibliographical) to make research of different kinds (demographic, archaeological, linguistic, environmental, ethnographic and iconographic) possible. Given the need to deal with the nature of cartographic evidence, we chose to provide Web mapping images of high resolution, offering the user a range of information on maps, the contexts of their production, reception and editorial manipulations. Also included are data on technical-scientific aspects (projections, scales, coordinates), printing techniques and material support that have made their movement and cultural consumption possible. This is a database that seeks to deal with cartographic information in its many facets: as part of the history of art and science, within historical, political, economic and social development, urban history, ethnography, ecology, etc.

The Digital Library of Historical Cartography was conceived by the Historical Cartography

Studies Laboratory team (LECH/USP). The site is a research tool which facilitates the gathering of relevant information for the registration of the production, circulation and appropriation of historical maps in their different contexts and media. The LECH team thought it fitting to give differential treatment to cartographic images, since the placing of digital maps on the Internet creates new dilemmas for researchers of ancient cartography. Each cartographic image is available along with extensive carto-bibliographical and biographical reference, technical, editorial and historical information relevant for cartographic documents analysis. The Digital Library was conceived to also trace data from similar sites constituting a useful research tool to gather relevant information [6].

II. DIGITAL LIBRARIES

As a reflection of our current cultural context, the printed collections are changing to meet the enormous challenges of the information technology era, adding digital spaces to their collections. The document concept has taken on new meaning with the inclusion of hypertext and new media in the everyday life of libraries that have to live with users, or groups of users-that demand dynamic, personalized content. This new generation of users finds it easy to use Internet resources, especially interactive communication, such as Web 2.0 [7].

The information explosion has boosted the emergence of new information technologies which have created a virtual space with previously unthinkable peculiarities for mankind. These technologies allow the use of electronic resources that promote the improvement and ever-growing speed with which information is transferred. Thus, the resources for the access to, and dissemination of, cooperation regarding the diffusion of knowledge are being constantly enhanced, especially in the academic area.

Within this context, digital libraries are already part of the agenda of leading universities, research institutes and organizations devoted to education and culture [8]. The availability of rare books, in a digital format to a wide audience, that could not otherwise be handled, except by specialists, is an invaluable tool for cultural improvement. [9]. The fact that digital libraries are a means of providing universal access and visibility, thus publicizing collections or cultural events the knowledge of which was previously restricted to their own respective communities [10, 11], is worth highlighting.

Regarding the analysis of historical maps, there is now a growing number of institutions developing digital collections, making these maps available to anyone with an Internet connection. Some collections are being developed as clearinghouses for those who might not otherwise have the opportunity to read or use the maps, targeting not only the most sophisticated researchers of academic communities, but also the general public, for their personal or professional use.

Preservation concerns and accessibility affect the decisions made as to which materials should be added to the collections of digital maps. Instead of a physical wear-and-tear, there is now a "virtual" wear-and-tear of these rare and fragile artifacts. Many of the resources in special collections are unique and irreplaceable. Because of their unique characteristics, their preservation, digitization and availability on the Internet should be a top priority for the library and in many cases should be part of the respective institution's strategic plan.

As there is still no consensus regarding the techniques and formats for digitizing historical cartographic material, a broader discussion on the criteria to be adopted for the selection of the maps to be digitized has become necessary. The philosophical aspects, such as the importance of the statement and the likelihood of use, and the more practical aspects such as physical condition, ease of scanning, preservation etc., need to be considered [12]. The participation of a multidisciplinary team of professionals, the standards to be adopted and the possible solutions to the problems involved in scanning are other aspects that should be included in the discussion.

III. PROJECT DEVELOPMENT

The conception of the Digital Library of Historical Cartography was developed by the Historical Cartography Studies Laboratory team (LECH) of the Jaime Cortesão Chair of the Philosophy, Literature and Human Sciences

Faculty (FFLCH/USP), and was carried through by the Informatics Center of São Carlos (CISC/USP).

A multidisciplinary team was put together to specify the requirements of the new public digital library. Live and remote meetings were held and a discussion list including all team members was created to foster interaction. The multidisciplinary integration carried out the possibility of building a database tool able to interact with the University's Bibliographical Database (DEDALUS) [13] as well as to retrieve information from other databases, not only from the University but also in other available Internet databases.

After analyzing the collected information, the new database was designed to gather all information and to be easily queried. At the same time, an intranet web site was developed to allow the LECH team to insert and update the collected information in the database.

One of the basic requirements was defining how to present high-resolution maps with a low cost to the network bandwidth. A careful research for adequate image formats was performed, not only to satisfy this requirement but also to preserve the original characteristics of the map. As a result, both free and paid software were chosen to convert the digitalized files into adequate formats for Web distribution. To allow for new, future formats, the Web system was conceived to allow easy integration of output drivers.

The second step was specifying the requirements and functionalities of the new Digital Library: Which indexes should be available to visitors? Which map data should be displayed? How should each map be linked to the available indexes and other sites? Which map data or detail should anchor those links? How can several digital objects from the same map on the screen be presented?

Finally, the CISC team also used a technique developed by Zoomify, Inc. [14], to present high-quality images in a fast and easy way over the Internet, that we call here the *Zoomify format*. This technique splits the image in small JPEG images in different levels, creating several image matrixes, which are browsed more quickly than the full high resolution image over the Internet and displayed to the user creating the illusion of a perfect zoom effect.

Some data available in the maps can be related to the present day world, to legitimize their historic and cartographic values. Therefore, these maps were geo-referenced by a specialized professional and inserted into i3Geo [15], an open source map file server developed by the Brazilian Ministry of the Environment, based on MapServer [16]. All files are stored in a storage file system. Each map has its own directory and a subdirectory is created for each digital object of the same map to be easily retrieved when required.

We have worked with the Santos Bank's map collection and Admiral Max Justo Guedes' carto-bibliographical information which is a cartographic inventory prepared by Admiral Max Justo Guedes. It is a universe of 2,000 handwritten sheets with accurate and erudite information about cartographic and bibliographic production from the fifteenth to the nineteenth centuries, prepared by the renowned scholar of Luso-Brazilian cartography [17].

The aim of this study is to guarantee open, public access via the Internet to the maps in the collection and make them available to users everywhere, whether through the Digital Library of Historical Cartography, or by means of DEDALUS. We believe it is important to increase public access to collections that were often treated as treasures, and therefore have been blocked to protect the institutional assets or treated as objects rather than as the sources of information they really are.

IV. RESULTS

To achieve the objective of this project, two databases of the University of São Paulo, the Digital Library of Historical Cartography, and DEDALUS, the Bibliographical Database, were used. The first step consisted of filling out a worksheet at the Digital Library of Historical Cartography (Fig. 1). At this stage the historiographical data available on each map

and from other sources were given priority (Fig.2 and 3).

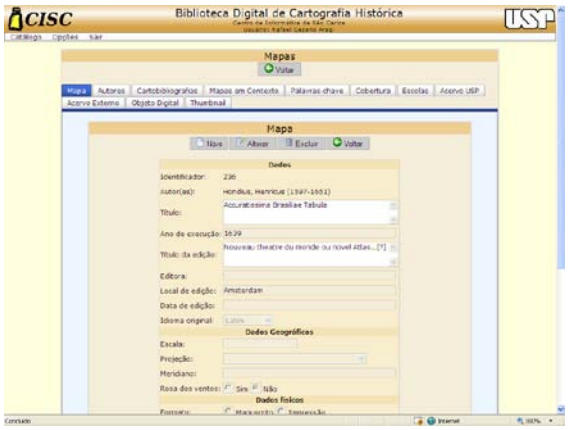

Figure 1. Screen of a record worksheet

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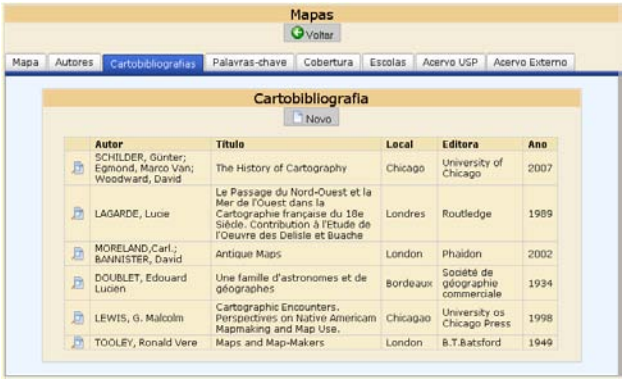

Figure 2. Screen of carto-bibliography

.

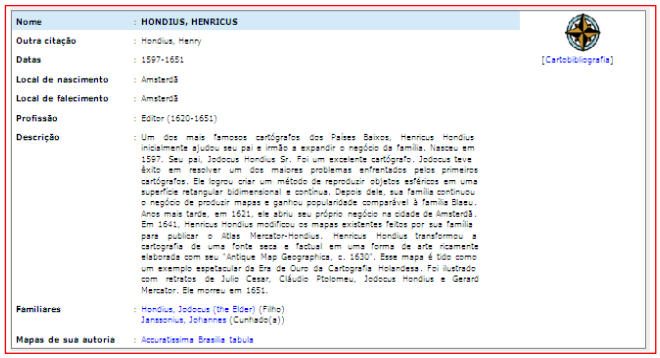

Figure 3. Screen of an author record (public site)

.

The second step called for the creation of the bibliographic record in the Bibliographical Database, when the data were recovered from the Digital Library of Historical Cartography in accordance with the specifications of the MARC format (Fig. 4) within the following fields: statement of responsibility (designer, cartographer, geographer), title, mathematical data, edition, publication, physical description, notes (cartographic school, Meridian, coverage etc.). In this phase, the bibliographical data of the map were given priority, in accordance with the specifications of the Integrated Library System (SIBI/USP). In addition to bibliographical data, links to the record and the map image are also inserted in the Digital Library of Historical Cartography. The image of the map displayed on the Web requires no plug-in.

Then the relationships involved were defined: inclusion of carto-bibliography, inclusion of links for quick viewing on the Web, download links to the images of maps in different formats: Zoomify (Fig. 5), JPEG, JPEG2000, SID and PDF, and information as to where to find the same map in other collections. When users search on DEDALUS for any of the maps available at the Digital Library of Historical Cartography, they have access to all the available resources (Fig. 6).

Figure 4. Screen of a DEDALUS record worksheet (MARC format)

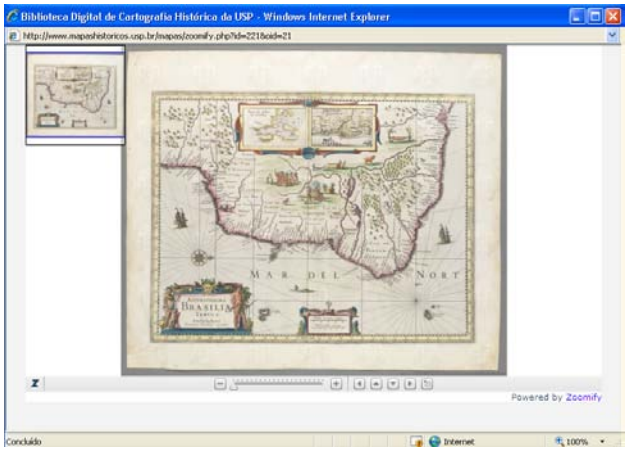

Figure 5. Screen of a map (Zoomify)

.

Figure 6. Screen of a DEDALUS record (public site)

. .

The last link on the right side provides other links related to the same map available in DEDALUS or in other University's sites, as well as links available on external libraries or sites in the Internet (Fig. 7).

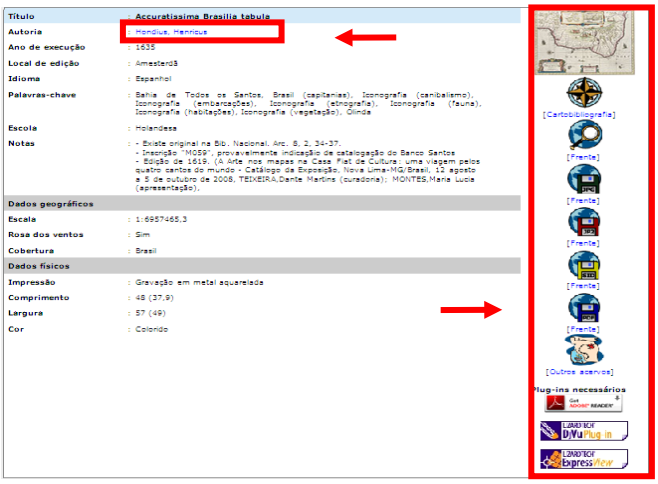

Figure 7. Screen of a record on the public site

In its first version, 50 maps are publicly available, accompanied by the detailed technical information and metadata. We developed indexes for the subjects, biographies, geographical coverage, iconographies and carto-bibliographies that will improve visitors' accessibility. In addition to cataloging each map on DEDALUS, we concentrated our efforts on the research of the contexts of production and reproduction of images at different times. The site seeks to register data about different authorships, and forms an image of appropriation and circulation that allow a less naive approach of cartographic documentation.

Users can explore the collection using indexes for titles, authors, execution dates, subjects, geographic areas, and schools of mapmakers. Also, information can be retrieved using a simple or an advanced search in the database. A gallery of digitalized map is also available (Fig. 8).

Figure 8. Screen of the Digital Library of Historical Cartography homepage

V. FINAL CONSIDERATION

Among the challenges we face at the moment, we should be aware of the dangers of filterless surfing. This situation threatens the credibility and reliability of the cartographic documents transmitted in cyberspace. There is a consensus among scholars that browsing on the Internet requires higher cognitive skills, linguistic acuity and erudition on the part of its users to filter, discriminate among and discard irrelevant data and the possible inconsistencies that populate the entropic labyrinths of cyberspace.

These questions guided the modeling of the Digital Library of Historical Cartography, which was developed on the basis of the supposition that the rare maps and/or books (atlases, nautical routes, and geographical descriptions) could be integrated into the database. The LECH team is responsible for tracking the reproduction of the printed and/or handwritten cartographic sources available in the different digital libraries, and for making the connections that generate new knowledge. Obviously, at this stage, such links form part of a team's preliminary work, but it is with the goal that in the future the users will be able to add data to the Digital Library of Historical Cartography, as well as use geo-referencing technology for the better treatment of the information contained in the maps, thus providing greater accuracy in the analysis of this peculiar type of research source.

The Digital Library of Historical Cartography is accessible not only to the historical cartography researchers, but also to students and the general public; beyond being a source of information about maps, it seeks to be interactive, exchanging information and seeking dialogue with different branches of knowledge [18].

The first version of digital library was written only in Portuguese. We plan on turning it into an international digital library in three other languages: English, Spanish and French. Also, new functionalities will be added, such as the context map, where visitors can read texts about a map, which were written by specialists from different knowledge areas after analyzing it. With this functionality we intend to encourage the use of maps in the classroom. Having analyzed the maps, we found important information that can be geo-referenced today in a world map. Therefore, we are now creating a GIS database to be integrated to the digital library.

ACKNOWLEDGMENTS

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Complex Systems as a Basis for Education and Pedagogy in the 21st Century

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Abstract *— Pedagogy as a science of education must be epistemologically grounded on complex systems, being a contemporary scientific paradigm that explains the processes of teaching and learning based on a neural network that integrates electrochemical, biological, genetic, and social elements in a complex reality that is surrounded by uncertainty, indeterminism and emergences resulting from the constant interconnectivity and which can be represented by complex mathematics such as constantly changing nonlinear dynamic behavioral patterns. These patterns cannot be established just by looking at the student's neural circuit, but as a result of the inter-cerebral dynamic between the professor and the student. The professor plays now a new role as detector of emergences and as creator of learning scenarios for unstable and trans-disciplinary contexts, while designing pedagogical processes grounded in non-classical logics that enhance the development of the student within the framework of complexity.*

Keywords: Complex systems, education, emergences, neural networks.

INTRODUCTION

The world goes through a complex set of changes at the social, economic, political, cultural, ecological and scientific levels, which are focused on instability, probabilities and indeterminism. At the same time, this scenario implies an education system immersed in the same dynamic by moving in different levels of complexity.

So far the educational and pedagogical processes have been planned and developed for stability and certainty, but the education of the future has been oriented towards probable states (uncertain ones), into the unknown, where the university professors of different disciplines must be prepared to move and manage volatile and uncertain contexts. Therefore, it is necessary to develop an epistemology that responds to the demands of reality and to the current knowledge of society.

Education and pedagogy as a streamline science should start from the understanding of educability processes, grounded in the complexity of the neural network and its nonlinear and uncertain connectivity, in order to design effective didactic and learning scenarios.

TOWARDS A NEW EPISTEMOLOGY OF EDUCATION

To manage unstable contexts, education and pedagogy in the 21st Century must respond to the needs of current society and the logic of postmodern thinking. According to Vattimo, "it is determined by the fruition, and it opposes to the functionalism of modernism, with a radical rejection of the instrumentation of the reason, focused on the vividness of each moment, as a presentist aesthetic that goes beyond fixed principles or criteria, determined, founded once and for all. (...) A thought that focuses on openness, on the dislocation of what had been consistent; it breaks the established methods and allows the search for dissent and instability as the authentic human [1]."

Therefore, it requires an education that responds to the complexity of current society through models, methodologies and pedagogical tools that are epistemologically based on contemporary paradigms. That is, on a dominant paradigm valid for this historical moment, with an explanatory power that satisfies the scientific community according to the current perception of reality [2].

For Zidane, “this current phase of paradigmatic shift, transitional stage in which we live, can be defined on the basis of uncertainty. After the era of continuous progress, of faith in the infallibility of science, the human being rethinks the complexity of reality [3].”

Educational knowledge must move beyond being a pedagogical knowledge based on a historical-philosophical reflection of past centuries. This is because, although the history of teaching and pedagogy is an essential element to understand the educational process that “allows to determine the purposes that should be pursued by education in every moment of your time [4],” the contemporary world requires pedagogy to go further and to work as a science applied to education; that is, to build their own theoretical and epistemological autonomy. It cannot continue denying the scientific nature of education, which is constituted as a science "as it tries to capture or grasp the complex phenomenon of education [5].” This implies, according to Foucault, the understanding of different thresholds of scientificity. This is why the scientific speech must define "the axioms that are necessary, the used items, the propositional structures that are legitimate for it and the changes accepted by it [6].”

Pedagogical knowledge has been developed through pedagogical models, but these have been intended to regulate and standardize the educational process by defining what, who and how to teach in order to shape qualities and virtues. However, their “main purpose is not to describe or penetrate into the essence of teaching. And, it is this normative character which differentiates their essence between knowledge models and scientific knowledge. Pedagogical models become then, epistemological obstacles because normative speeches cannot account for cognitive speeches (....). A language of level of differentiation and inferior cognitive hierarchy cannot explain or communicate complex messages of qualitatively superior order.” The contemporary scientific models are heuristic models based on the creation of new roads and rely on logic, cybernetics, mathematics and problem solving simulations. Therefore, it considers that traditional pedagogy based on a "naive theory of knowledge, is not in a position to contribute to the translation of cultural scientific thoughts and their creation processes to the contemporary context of the students [7].”

However, pedagogy as a science of education must respond to today's society of knowledge because “the scientific model on which our civilization rests has been changing since the advent of the theory of relativity, quantum physics and the laws of thermodynamics. From all these fields of scientific knowledge, comes a new vision of the world that transforms humankind. If before the human being was looking at himself as the center of the universe, today he finds himself as the consciousness of the biosphere (Lovelock's Gaia hypothesis), as an observer of the world (Einstein) and even as a creator of reality (Schrödinger). Thermodynamics gave the western men back the freedom and the role of evolution (Prigogine) that had been kidnapped by Newton's mechanistic [8],” which means that the reality and the dynamic of today's world require a new science to explain it, a new thought to confront it, a new rationality and therefore, a new educational system to energize it.

Within this framework of contemporary science, a new paradigm must emerge to create normal science, which becomes a new relative truth [3] that explains reality by

allowing the construction of new educational knowledge.

The emerging paradigm of complex systems that is part of a category and that configures complexity as science, tries to explain the world in an eminently scientific work focusing on: dynamic, changeable and mutable systems, together with the study of concepts such as attractors, chaos, and rupture of symmetry and bifurcation, nonlinear logic, simulation, probabilistic behavior, artificial intelligence, artificial life and study of emergent phenomena, among others . These systems must acknowledge the existence of dialogue among biology, physics, mathematics, logic, information theory, psychology, neurophysiology and philosophy and many others, while providing the basis for transdisciplinarity [9].

The educational process is unpredictable and presents changes not previously envisaged. It is non-linear -as some have sought to state-; each class is different, full of new aspects and unforeseen situations derived from elements with highly complex variables such as genetic, social, cultural, biological, cognitive, and psychological ones. Educational theories are superficial and based on order, structure and everything that it is considered to be consistent. Therefore, they differ from what actually exists in a complex reality of educational practice –which is changing, unexpected and different in every individual and in every group of students.

It cannot be otherwise because, unlike traditional science, the epistemology of social and human sciences is currently based on incompleteness, uncertainty, and on the chaotic relationship between order and disorder. And education as part of this context must be conceived that way. Therefore, the epistemological grounds of modernity must be reconsidered and its educational narrative must be rebuilt because "the only reason that can be accounted for in educational phenomena is the complex reason [10].”

In order to achieve this it is necessary to establish the teaching-learning processes that are rooted not only in an epistemological positivist vision, behavioral and linear (empirical-analytic type), and also in social-critical approaches or historical-hermeneutical but it should go even beyond the contextual and relational, conceiving reality as a complex system surrounded by uncertainty, randomness, indeterminism, nonlinearity, chaos, constant change, and the interactions and emergences that are beyond any prediction or traditional scheme.

This approach deserves the support of a new education oriented by non-classical logics, and the development of heuristics and metaheuristic tools in order to understand nonlinear dynamic systems [11] and thus being able to address the new education landscape issues.

Contemporary university dynamics remain linear and rigid, based on determinism without responding to the dynamic that has been shaping the production of knowledge and progress in various disciplines, evolving into a gap between current scientific development and educational processes. This is the case of engineering, where there have been great advances in knowledge production on the basis of complex systems, but educational systems are still developed using parameters of past centuries. Science must be taught, epistemologically speaking, under the same fundaments by which knowledge is produced when looking for a meaningful learning of the discipline, because the same logic that is applied to the production of knowledge should be used when this knowledge is taught. This gap between production of disciplinary knowledge and pedagogy has been historically shown to society because “pedagogical conceptions are delayed with respect to social changes (political, economic and cultural), implying that there is a disconnection and a gap between social phenomena and educational phenomena [12].” The reason is that university teaching in the different sciences

has been conducted, in most cases, empirically (only with the knowledge of the discipline but without educational training or teaching) and also, the lack of pedagogical training and research in education responds to paradigms used out of context.

Paradigmatic understanding in education is essential when considering that paradigms respond, according to Guba (1990), to basic considerations of different types, such as: ontological on the nature of reality, epistemological about the nature of the relationship between the researcher and the discipline's known object. Also, these paradigms clarify the methodology to produce knowledge [13].

COMPLEX SYSTEMS, EDUCABILITY AND NEURO-LEARNING

Pedagogy as a science of education, systematizes the pedagogical knowledge with its main concept, educability of the student, which studies the human being as a subject of education, by asking not only how they learn, but also by considering how humans develop their skills in different human dimensions such as: cognitions, attitudes and values (the ability to be formed) [14]. This educability has its biological roots in the brain and its neural networks (like a complex system with many interactions in which multiple possibilities emerge, energizing brain plasticity). And, it is in the understanding of the complexity of these systems that neurological teaching, science, and their different educational areas must be based.

When approaching the study of the brain within the framework of educability as a complex system, it must be considered that these systems are, in general, cyclical self-organized structures that streamline genetic, informational, biochemical, energetic and thermodynamic processes. Then, these systems extract energy from the environment in order to grow, maintain and expand their shape while working, processing data, exchanging information, and building themselves. Finally, they transform energy and release heat and thermodynamic waste (entropy) into the environment (driven by flows of energy), behaving like systems with an organization that depends on the entropy released around, the environmental gradients and their interaction in a non-thermodynamic equilibrium [15].

The brain is a complex system, structured by a large neural network which, on a genetic basis, has an electrical intrinsic activity and permanent chemistry and flexibility, with intermittent oscillatory exchanges among different groups of neurons (that can oscillate or not at some point, depending on multiple variables that emerge from the electro-chemical interaction). Even when facing the same signal, different aspects can be perceived or encoded. These neural networks resonate not only with one another, but also with distant groups, generating a swing phase, in which disparate elements work together as if they were one (in an amplified way which allows them to travel great distances). This resonance, oscillatory neuronal consistency and concurrency, generated by electro-chemical activity, determine the root of cognition and learning [16].

According to Ramon y Cajal, learning processes are set by electric flows through brain cell membranes, strengthening their ability to generate new synaptic connections [16].

Memory also plays a part in that neuronal electrical activity. The ones in the same neural circuitry determine short-term memory (Coldman- Rabice 1996) by generating an activity that produces a synaptic feedback with activation of neuron's intrinsic properties (Camperi and Wang, 1998). Long-term memory can also be determined by associative circuits that determine long-term potentiation (LTP) [16].

The activity of the circuits that determine memory are very fluid and in turn determined by changes that occur in the synapses, which also have the ability to modify the amount of

neurotransmitter released by a potential action, producing receptors that make the cell more sensitive to LTP or less sensitive to long-term depression (LTD) [16].

In short, the brain function has a closed system which is responsible for the subjectivity and semantics, and an open system, responsible for the sensorimotor transformations that relate the private component to the external world (Llinas, 1974.1987) [16]. However, there are situations in which certain properties of the external world define the intrinsic central connectivity as in the case of perceptual learning (Bateson 1996) [16].

These complex neural networks process cognitive, emotional and learning elements, also mediated by the constant interaction of multiple neurotransmitters such as: noradrenalin (located in the brainstem and ending in the amygdale, hippocampus, thalamus and hypothalamus) which acts in the cerebral cortex by modulating the cognitive functions of the brain; dopamine from the brain stem, which acts in the brain stem and cerebral cortex; acetylcholine (in the neocortex, the amygdale and hippocampus); amino butyric acid (from the hypothalamus and reaching the occipital and frontal area) and serotonin, which acts widely in the cerebral cortex, among others [17].

Additionally, the brain system is modulated by hormones secreted by the hypophysis such as oxytocin, vasopressin and ACTH, as well as peripheral hormones such as adrenaline or endogenous opioid peptides such as endorphins [17].

Learning depends on brain plasticity, which is determined by changes in the structure and functioning of synapses. The synaptic efficacy depends on the early ontogeny in the formation of synapses, of the tuning of new synapses (which depends on adequate stimulation), and finally, of the synaptic regulation which lasts over a lifetime and which has a direct relation with experience. This constant and dynamic interaction of genetic processes of maturation and learning will shape the student's behavior and learning. [17]. For instance, "neural circuits equipped with fast plastic mechanisms from the hippocampus and from other medial temporal lobe components, make this region particularly suitable for associative learning [17]."

Although structural changes are determined by synaptic connectivity, it is the local characteristics of these connections – given by the molecular changes– which determine the effectiveness of these connections and "can drastically modify the operating mode of large neural networks [18]."

The brain system may also be modulated by conditions such as stress, where peripheral endogenous hormones are released or by contextual situations where learning occurs by the discharge of neurotransmitters, hormones and endogenous opioids, facilitating or interfering in the process with motivational or affective elements [17].

The dynamics of electro-chemical connectivity within the brain network is performed under a complex system as follows: "The human brain consists of more than $10^{\wedge 10}$ million and perhaps more than $10^{\wedge 11}$ neurons (tens of thousands of millions), where each of them receives multiple contacts from other neurons and in turn connects with other many cells; the combination of possible interactions is more than astronomical (...). This activity also produces multiple changes in other parts of the body, such as in the sensory cells of muscles and in areas of contact with the medium through interneurons that interconnect them. Thus, in the human body about $10^{\wedge 11}$ (one hundred billion) interneurons connect some $10^{\wedge 6}$ (one million) motor neurons that activate a few thousand of muscles, with about $10^{\wedge 7}$ (tens of millions) sensory cells distributed as receptor surfaces along the body. Between the motor and sensory neurons, the brain interposes as a giant tumor filled up with interneurons that interconnect with one other (ratio of

10/100,000/1) in a constantly changing dynamic [18].

This magnitude of interconnections generates an infinite number of possible situations. In fact, “given that there may be an unlimited number of possible states within this network, the possible behaviors of the organism may also be virtually limitless"[18]. Therefore, the emergences that arise will always be dynamic and changing, under uncertainty, randomness and nonlinearity (disabling any linear mathematics and forecasting, and always considering them exclusively within the field of probabilities). Therefore, neuronal connectivity has a chaotic feature or nonlinear dynamic properties that change continuously.

Living systems respond to external influences with structural changes that affect their behavior, adapting structurally to their environment, and resulting in a structure that holds the previous structural changes or past interactions. These systems react to the environment by coupling with structural changes, according to their nature and organizational pattern (non-linear) of unpredictable behavior. This structural coupling determines intelligence, learning and behavior [18].

These structural changes can be triggered by interactions with the environment or as a result of the internal connectivity dynamic, which is constantly changing. But this ongoing transformation of the structure does not entail disorganization.

The environment and the internal network generate reciprocal perturbations. In this interactive dynamic with the environment, the neural network classifies the disturbances or sees them according to its current (in that precise moment) structure [18]. That is, "in these interactions, the structure of the environment only triggers structural changes in autopoietic units (not determined or instructed) and vice versa for the environment. The result will be a history of mutual structural changes, that is consistent when not disintegrate: there will be *structural coupling* [18]. The nervous system of an organism changes its connectivity with every sensory perception [19].”

The nervous system as an autopoietic system provides continuous structural changes that determine plasticity, but retains its full identity or pattern of network organization (despite the fact that these network components are produced and processed continuously, renewing and regulating themselves) [19]. "The neurons, the body that integrates them, and the environment in which they interact, operate reciprocally as selectors of their respective structural changes, and couple structurally with each other: the body operator, including the nervous system, selects the structural changes that allow it to keep operating, otherwise it will be disintegrated [18].”

Learning is an expression of the structural coupling [18]. Interactions of the neural network “allow the generation of new phenomena by allowing new dimensions of structural coupling [18].”

The nervous system is involved in cognitive phenomena by "opening up new dimensions of structural coupling for the body, by enabling the association of a variety of internal states in the body with the diversity of interactions in which it can enter [18].”

NEURAL NETWORKS AND PATTERNS

This dynamic of neural circuit connectivity originates intricate patterns of interconnected frames that establish nonlinear relationships, determining stimuli or messages that become cyclical feedback loops, with the ability to regulate themselves [19].

The neural network is determined by complex internal patterns that must be represented on an abstract geometrical space in the brain [16]. This type of pattern responds to “a configuration of characteristic relationships within a given system [19].”

The self-organization of complex structures develops a stable state, which however, is distant to the balance (different from one in balance such as a crystal). Those are dissipative structures that evolve in instability, transforming themselves in structures of increased complexity [20]. “A seemingly complex and chaotic behavior can lead to ordered structures, to subtle and beautiful patterns [19].”

Nonlinear interconnectivity of networks and self-organizing systems has been only modeled through the mathematics of complexity or theory of nonlinear dynamic systems [19]. This mathematic is one of relationships and visual patterns, known as topology or elastic geometry in which figures can be converted into other figures [21]. That is, they belong to ordered patterns that correspond to chaotic systems.

This kind of mathematics can map solutions –curved or graphed shaped– by using computer systems [19]. These patterns represent an abstract mathematical space, known as phase space [20]. There, patterns can be represented in the space by open curves that close themselves in spiral towards the center like strange attractors (because of the attraction towards the center), which are specific to chaotic systems. They never repeat themselves, covering new regions of phase space by forming highly organized complex patterns [19].

These paths help transform random and uncertain data into visible forms. The path may contain thousands of points and multiple variables but its movement is represented in a low dimensionality and still, it is impossible to predict the point of phase space where the path will pass by [19].

These attractors lead to an abstract region of space called basin of attraction. These patterns favor the non-linear structural analysis of complex systems by identifying and classifying themselves accordingly to their characteristics in a comprehensive scheme called phase portrait [21], which allows analyzing features of complex dynamic problems that outweigh any prediction.

Phase portraits can disappear or change and new attractors will appear because either critical points of instability act, or bifurcation (catastrophe) points change the phase portrait by giving a new pattern or order [22]. Then, the new paths that are open by bifurcations, even when determined by the history of structural coupling, are unpredictable [19].

The structures of chaotic attractors can be described with the mathematical language of fractal geometry, language used to describe and analyze the complexity of the natural world (clouds, mountains, lightning) [23].

In fractal language, each piece is a reduced-size copy of the whole (a kind of holographic approach). Strange attractors are examples of fractals –multilevel structures with the same patterns. In fact, "strange attractors are paths in phase space that exhibit fractal geometry [19].”

The stated above is important because, although it is impossible to predict the value of variables, “the qualitative characteristics of the system’s behavior and the degree of blunting can be predicted [19].”

The interaction of the nervous system with the environment –with the constant modulation of its structure through abstract patterns in space– generates a cognitive process that is always accompanied by emotions, feelings and bodily processes that determine intelligence, memory, learning and decision making.

INTERCEREBRAL CONNECTIVITY

The neurological dynamic that has been revised so far with emergent patterns, has been established at individual levels (a brain without any external interaction), but when it comes to interaction with another person, a neurological intercerebral connection is produced –a nervous bridge that allows to impact the other person’s brain and vice

versa–, while generating positive or negative situations of cognitive, biological, emotional, immune or genetic type in both systems. These interactions “affect our brains and our biology [24].”

Interactions with other people reshape brain neuroplasticity (size, number of neurons and synaptic connections) [24].

This has to do with the activation of specific neural cells such as spindle cells and mirror neurons. That is, the brain, through “neural circuits, commands our interactions.” It creates a resonance between mental patterns and mental maps known as shared reality [24].

COGNITIVE DYSFUNCTION AND SIGNIFICANT LEARNING

There are situations in teaching and learning processes that encourage the use of the maximum mental capacity with a bit of pressure, leading optimizing attention, memory and performance .But when this pressure is excessive (depending on the student’s susceptibility, and his or her neurohormonal and electrochemical responsiveness) stress, fear and anxiety are triggered, determining a cognitive dysfunction where hormonal axes are shot and biological changes take place. The amygdala triggers circuits that affect the function of the prefrontal cortex and a negative impact on hippocampal neurons occurs (the key organ of learning and neurogenesis). Soon processes of learning and memory are interfered, because automatic emotional responses have been fired, decreasing attention, concentration, memory, creativity, learning capacity, performance and the ability to make decisions and solve problems in students [25][26]. There are also conditions such as sadness and boredom that generate discouragement and difficulties in cognitive functions and learning. In order to make learning processes enjoyable, states are required to be optimal. Feeling well and calm determines how neural networks that control the mental processes can be more efficient, faster and operate at its maximum performance [27]. Pleasure and tranquility go hand in hand with cognitive efficiency.

THE NEUROLOGICAL DYNAMICS OF INTERSUBJECTIVITY AND THE ROLE OF PROFESSORS

The ultimate goal of the teaching-learning processes is for the student's brain to reach an efficient connectivity of his or her neuronal networks; integrating in this way cognitive, affective, communicative and social processes. To generate significant learning (not just rote-like, linear and behavioral), while developing creative and innovative processes, critical thinking, the ability to solve problems and with the competence to learn how to learn and learn to live together. That is, to create a better human being for the complexity of current society.

With regard to the above, the following questions arise in the context of complex systems. What role does the professor play to facilitate the learning process in this context? How can the professor possibly activate the student’s brain to reach optimum levels of learning and creativity?

In this respect, this thesis has been established:

The professor's role is to identify structural patterns and emergences that occur in the interaction with the student as a result of intersubjective dynamics of intercerebral circuits. Also, the professor must modulate them and help the student's brain reach a state of optimal cognitive efficiency.

When the professor-student relationship takes place in different educational scenarios (classroom, tutoring, counseling, etc.), a neurological dynamic of intersubjectivity can be established under the structure of a complex system between both brains, as a product of this intercerebral interaction. This generates a number of cognitive and emotional situations in both professor and

student, which are represented in a phase space in the form of attractors or patterns that tend to be repeated and that can be received at the intellectual, emotional or physical level. These figures or models tend to be repeated if the stimuli are similar, but if the incentives are changing, new attractors or more complex figures of fractal type are generated in an abstract level. However, these are manifested in the reality of relationships at different levels.

Bifurcations or catastrophes of the patterns are being constantly generated by stimuli of the professor, the students or the context, creating new and unpredictable situations that can be perceived in the actors of the system by looking at their cognition or affection and which are manifested in its corporeality.

To potentiate the process of creativity, learning and problem solving, a special field is required, given by emergences derived from appropriate emotional states between the student and the professor. These states are the result of neurological dynamics of intersubjectivity among the actors.

The professor, therefore, is an essential part of the system, not as a giver of information, neither as applier of rigid and decontextualized models of education, but as a catalyst for neurological intercerebral networks that are activated between professor and student within a context of uncertainty and permanent change.

The professor’s goal should be to enable the student’s brain and his own to reach an optimal cognitive, emotional, social and emotional level with impact on the system. This role is completely different from the traditional one: linear, behavioral and authoritarian (attitudes that favor the appearance of patterns –fractals– not conducive to learning).

The emergence can also cause stress, boredom, or anxiety in the professor or in the student, situations that hinder the learning process for the student and, the teaching process for the professor.

The educator's role should be to identify, each time, patterns and signal of disaster or bifurcations when observing the context and the student at a verbal and nonverbal level, together with what is perceived at these levels. And, according to that, the educator should generate changes that affect the whole system, by designing learning scenarios suitable for uncertain and unstable environments and, by adjusting didactics according to the moment, attractors and emergences as they appear. Linear and pre-planned methodologies will not work because they are designed for stable contexts, not real ones. Educability must respond to a complex dynamic that transcends the forecast, the goals and objectives that are not achievable.

CONCLUSIONS

The focus of education in the 21st Century must be transdisciplinary and with new pedagogical models based on uncertainty, randomness, chaos, nonlinearity, emergence and permanent change; that is, based on complexity.

Pedagogy as a science of education must be grounded epistemologically in contemporary paradigms

Educability is grounded in the brain and its complex neural network. On this basis, the learning processes and contemporary didactics should be designed

Although the educational process must focus on student learning, the professor is an essential part of this system and significantly affects the final result

Science should be taught, epistemologically speaking, on the same grounds on which knowledge is produced when looking for a deep understanding of the discipline, because the same logic that is applied when knowledge is produced should be used when this knowledge is taught.

The professor's role is to identify structural patterns and emergences that occur in the interaction with the student as a result of the

intersubjective dynamics of the intercerebral circuits. Also, the professor must modulate them and help the student's brain reach a state of optimal cognitive efficiency.

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Extract, Transform and Load Architecture for Metadata Collection

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Abstract *— Digital repositories acting as resource aggregators typically face different challenges, roughly classified into three main categories: extraction, improvement and storage. The first category comprises issues related to dealing with different resource collection protocols –OAI-PMH, web-crawling, web-services, etc.– and their representation: XML, HTML, database tuples, unstructured documents, etc. The second category comprises information improvements based on controlled vocabularies, specific date formats, correction of malformed data, etc. Finally, the third category deals with the destination of downloaded resources: unification into a common database, sorting by certain criteria, etc.*

This paper proposes an ETL architecture for designing a software application that provides a comprehensive solution to challenges posed by a digital repository as resource aggregator. Design and implementation aspects considered during the development of this tool are described, focusing especially on architecture highlights.

Keywords*:* aggregation, data integration, data warehousing, digital repositories, harvesting.

INTRODUCTION

Resource aggregation is one of the activities performed in the context of digital repositories. Its goal is usually to increase the amount of resources exposed by the repository. There are even digital repositories that are only resource aggregators – e.g. do not expose their own material.

Aggregation starts with relevant resource collection from external data sources; currently, there are several communication and transference protocols, as well as techniques for collecting available material from data sources that were not originally intended for this purpose. Some of these protocols and techniques include:

OAI-PMH [1]: A simple and easy-to-deploy protocol for metadata exchange. It does not impose restraints upon resource representation, allowing the service repository to select metadata format.

Web-Crawling [2]: A robot scans web pages and tries to detect and extract metadata. This method is useful for capturing the large volume of information distributed throughout the Web, but the problem is that documents lack homogeneous structure.

Web-Services: Using SOAP or XML-RPC as communication protocols in general,

resource structure depends on server implementation.

As briefly seen above, methods and means for resource collection vary significantly depending on the situation, context and specific needs of each institutional repository, both at the level of communication protocol and of data. Therefore, independent data collection processes and different analysis methodologies are critical to standardizing aspects such as controlled vocabularies, standard code use, etc.

Likewise, when it comes to determining the use of collected information, there are also different situations that depend on specific repository needs. The most common scenario is the unification of collected resources into a central database. Another usual approach is to logically sort information –i.e. by topic, source country, and language– inserting the resources in different data stores. Furthermore, it may be necessary to generate additional information by applying analysis and special processes to resources –concept extraction, semantic detection and ontology population, quotation extraction, etc– and use different databases to store this new information.

In general, information from different repositories is typically diverse in structure, character encoding, transfer protocols, etc., requiring different extraction and transformation approaches. Analogously, specific capabilities are required to interact with each data store that receives the transformed resources. This requires a set of organized tools that provide a possible solution. There are a number of potential complications: initially, it is necessary to find –or develop– a series of tools, each tailored to solve a specific problem, and then install, setup, test and launch each of them. Subsequently, there is the problem of tool coupling, and the need to ensure reliable interaction, since it is highly probable that these tools act upon the same dataset. On the other hand, it is important to consider the type of synchronization mechanism used to determine task sequences: order of tasks that each tool will carry out, which tasks can be executed simultaneously and which ones sequentially, etc.

From a highly abstracted viewpoint, it is possible to identify three main issues: Extract, Transform and Load (ETL).

DEVELOPMENT OF A UNIFIED SOLUTION

ETL [3] is a software architectural pattern in the area of Data Integration, usually related to data warehousing. This process involves data extraction from different sources, subsequent transformations by rules and validations, and final loading into a Data Warehouse [4] or Data Mart [5]. This architecture is used mainly in enterprise software to unify the information used for Business Intelligence [6] processes that lead to decision-making.

Given the challenges presented by resource aggregation via institutional repositories throughout the different phases in heterogeneous information management, a comprehensive ETL solution is highly practicable.

This paper presents the development of a tool intended as a unified solution for these various issues.

The design is based on the following premises:

(a) Allow the use of different data sources and data stores, encapsulating their particular logic in connectable components.

(b) Allow tool extension with new data source and data store components developed by third parties.

(c) Allow selection and configuration of the analysis and transformation filters supplied by the tool, encapsulating the particular logic in connectable components.

(d) Allow tool extension by adding new analysis and transformation filter components developed by third parties.

(e) Present an abstract resource representation for uniform resource transformation.

(f) Provide a simple and intuitive user interface for tool management.

(g) Provide an interface for collection and storage management.

(h) Achieve fault tolerance and resume interrupted processes after external problems.

(i) Provide statistic information about process status and collected information.

The software tool was developed along these premises, trying to keep components as separated/uncoupled as possible. Fig. 1 shows an architecture diagram for the tool.

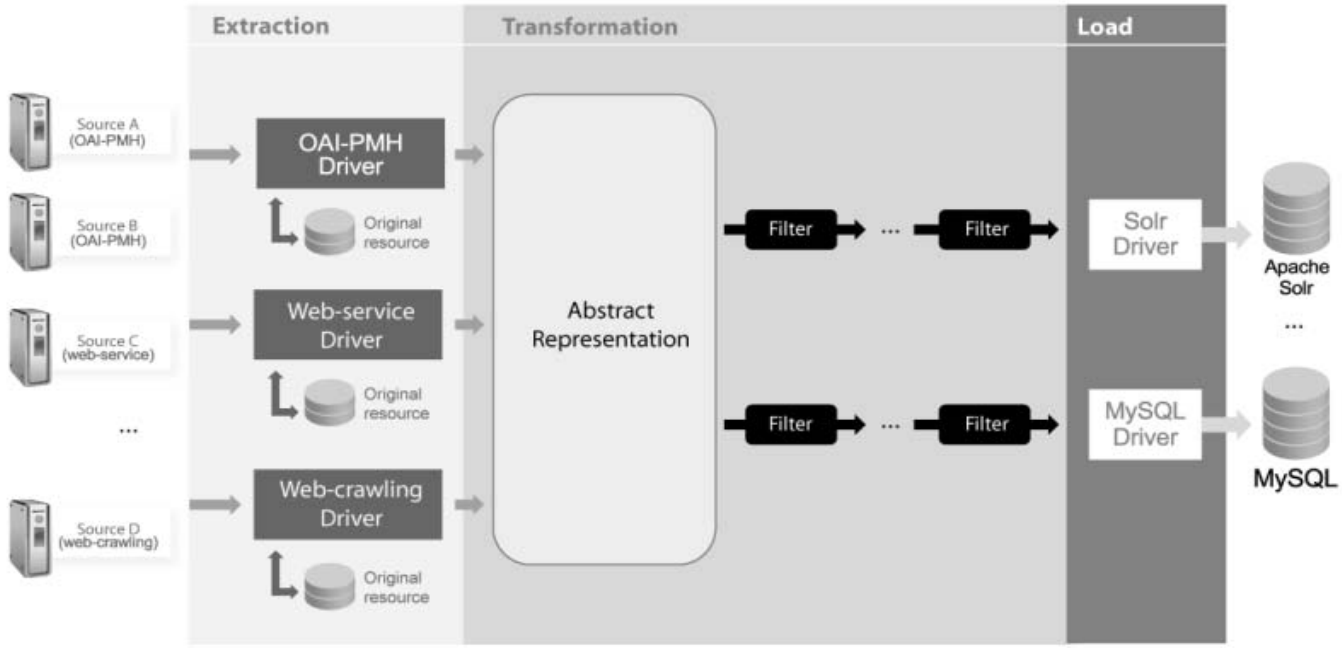

Figure 1. Architecture diagram

DATA MODEL OVERVIEW

This data model is primarily based on three elements, from which the whole model is developed. These elements are Repositories, Harvest Definitions and Collections.

Repositories represent external digital repositories with relevant resources, thus being the object of data collection. A repository is an abstract entity that does not determine how to obtain resources and only registers general information such as the name of the source institution, contact e-mail, Web site, etc. In order to harvest resources from a specific repository, connection drivers –components with the required logic to establish connections– must be first associated, determining the relevant parameters.

A *Harvest Definition* element comprises all the specifications required to carry out a harvest instance (or particular harvest). That is, harvesting processes are performed according to the harvest definitions in the adequate status –i.e. still have jobs to carry out. A harvest definition is created from a connector associated to a repository, thus specifying the protocol or harvest method used. This allows the creation of multiple harvests on a single repository, using different communication approaches.

Collections are the third important element. They represent the various end targets for the information generated after applying transformation and analysis processes to harvested resources. As is the case with repositories, collections are an abstract element within the system, and this means that each collection has an associated connector that determines the storage method and its corresponding parameters. The main goal is to allow the use of the different storage options, not only based on the storage type, but also the type of information to be stored. For example, let us consider a collection that specifies storage into the file system as backup, another collection that specifies insertion into an Apache Solr [7] core for resources identified as Thesis, and a third collection that specifies insertion into another Apache Solr core for resources written in Spanish.

The data model is completed by the three main elements described above, adding elements associated to connectors and to harvest definitions, supplementary information about repositories and additional elements for controlling and tracking harvesting methods.

EXTRACT

Extract is the first phase in resource harvesting, carried out in different stages. The first is the determination of harvest definitions that must be loaded in order to be run. For this purpose, each definition has scheduling information that specifies the date and time of the next execution. Since harvest definitions are the actual extraction jobs, they contain a reference to the interacting connector to establish the connection and download the information. Likewise, harvest definitions are narrowed down, adding supplementary information –usually parameters– about the associated connector protocol. Specifically, the connector is the component that carries the logic required to establish the connection, and the harvest definition specialization contains the particular harvesting parameters.

In some cases, harvesting jobs must be carried out in stages, due to a number of reasons: data volume is too large and thus must be partitioned, organizational issues, etc. An actual case is OAI-PMH protocol, which allows incremental harvesting by date range. This is shown in the data model, when harvest definitions are decomposed into *actual harvests*. For example, an OAI harvest can be created specifying a date range of one year and then split that harvest into one-month separate harvests, which will generate twelve harvests that must be completed to meet the requirements of the initial definition. This also reduces losses due to system crashes, since only the job associated to a part of the harvest would be lost, and not the whole harvest itself.

This fault-tolerance is achieved using *Harvest Attempts*. That is, for each connection a new attempt is registered, and it will remain valid until the harvest is completed or an interruption occurs, either by the administrator, a server timeout, errors in the responses, system crashes, etc. There is a configurable limit that determines the number of attempts to try before disabling the harvest.

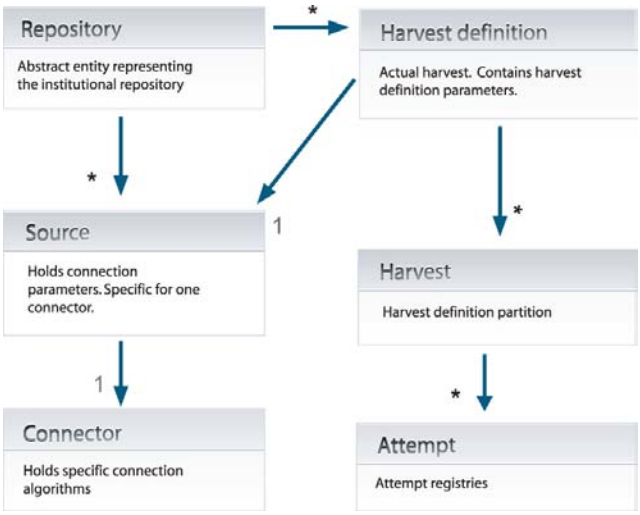

Figure 2. Extraction phase data model abstraction

Downloaded information is handled by a general handler common to all connectors which stores harvested data locally and retrieves them when needed. For example, a particular handler can store data as files on disk.

TRANSFORM

This phase initially transforms the harvested resources to a simple abstract representation that allows uniform processing of all resources. This transformation is done by connectors, since they contain information about the original representation and the rules that must be applied to take it to an abstract level. Each resource, already in their abstract representation, goes through a filter chain in order to analyze particularities and modify data, if necessary. The system comprises a predetermined set of independent filters, which are simple and reusable components that act according to parameters specified in a filter configuration file.

As seen above, each harvest definition refers to a target collection set. Each collection specifies a set of filters that must be applied before inserting a resource into that collection, where selection order determines their application.

Filter execution may lead to modification, adding or erasing specific resource data (metadata values); depending on specific filter functions and configuration.

Available filters on this application include:

- *CopyField*: Copies content from field to field. If the target field is nonexistent, the filter creates one.
- *DefaultValue*: Determines if there is a nonexistent or valueless field. If this is the case, it creates a new one with a predetermined value.
- *FieldRemover*: Takes a field list and removes them from the resource.
- *Tokenizer*: Takes field values and tokenizes them from a specific character series, generating multiple additional values.
- *Stack*: Aggregates filters; defines a filter list (with configuration and order) to ensure the order of application.
- *ISOLanguage*: Applied to a field that specifies the resource language, searches for the field value in a language list and replaces the original value with the ISO-639 language code found.
- *YearExtractor*: Applied to a field that contains a date, extracts the year and saves it on a new field.
- *Vocabulary*: Takes field values and contrasts them against a dictionary, unifying word variations and synonyms into a single word.

LOAD

This is the third part, when transformed resources are sent to data stores, completing the scope of this tool. For this purpose, each

collection refers to a target connector that contains the data store logic required to interact with this latter.

After going through the transformation stage, resources in their abstract representation are sent to the connector associated to the target collection, where they undergo further transformations to produce an adequate representation that matches data store requirements.

MANAGEMENT

Loading of repositories, collection, harvest definitions, filter selection and so forth is managed through a web application. This web application is included in the software and allows management capabilities to handle all aspects that make up the tool. More precisely, it allows management of collections, repositories, harvest definitions, connectors –source and target-, languages, publication types, users, roles, system parameters, collection assignments in a harvest definition, filter selection from a collection, among others. Besides, it has a special section to control the execution of collection and storing, from which these processes can be independently initiated and interrupted, creating a real time report of the jobs that are being run.

Finally, simple reports associated with repositories are created to show the status of completed harvests -number of failed harvests, number of harvests with no register return, etc. - average daily resource downloads, total volume of document downloads, and more. Analogously, resource distribution by source target is shown for each collection, specifying amount and proportion represented by each one in the whole collection.

FUTURE RESEARCH

This tool has a number of features that allow for further improvements or extensions. Key aspects include:

Transformations: The most important extension point seems to be focused on transformations, since they allow the application of interesting processes to the collected information.

Semantic extraction: Detects relations among resources based on the information they contain.

Fulltext download: Identifies an URL pointing to the fulltext and attempts to download the document, to apply further filters to its content.

Author standardization: Analyzes the author's name to generate standardized metadata.

Duplicate detection: Provides techniques to avoid insertion of two resources –probably from different sources- when they represent the same resource.

CONCLUSION

This document discusses a recurring challenge faced by digital repositories that arises from resource collection from diverse sources; then shows how an architecture used mainly in the business area can provide a solution for these issues. The three main ETL architecture phases cover each one of the activities performed during the resource collection work in the context of digital repositories, making it an adequate approach within this area, allowing for further improvements and extensions, as seen above.

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On Wafer Thin Micro Batteries: Micro-fabrication, Towards the Development of Aluminum-anode High Performance Cells

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Abstract *— Reduction in size and weight of micro-electronic devices becomes limited by the availability of suitable power sources. This paper presents micro-fabrication routes of an aluminum anode/oxygenated alkaline electrolyte/platinum cathode micro cell as a first step towards the development of highly efficient thin form factor aluminum anode cells. On-demand microfluidic addition of electrolyte can offer long shelf life. Several cell designs are made on a single wafer allowing for variation of the electrode area ratio; this ratio affects the aluminum anode utilization efficiency. Cell's open circuit voltages are in the 1.2-1.4 Volt range. Several geometries provide high current densities relative to the cell's overall size when subject~~ed~~ to small load resistances (up to 2 milliamps per cm^2). A preliminary comparison of anode utilization efficiencies (energy per unit gram of deposited aluminum) among fabricated cells with various platinum aluminum area ratios is presented.*

I. INTRODUCTION

The development of Micro-electromechanical Systems (MEMS) has enabled the design of portable sensor systems that require reliable powering systems of comparable sizes. Parallel development of small but highly efficient powering devices is required. Power-MEMS is still an area of active research and development [1-2]. Reports on micro and miniature energy environmental harvesting systems and thermal and combustion devices are common in literature [1-6]. A variety of electronic devices, from cell phones and lap top computers to medical devices rely on the use of batteries. A logical approach is the miniaturization of electrochemical cells [7-16] as a Power-MEMS option. Lithium-ion thin film batteries were one of the first systems to be investigated for the development of micro batteries [8-11]. Fuel and semi-fuel cells are also subjects of miniaturization [12-14].

Microfabricated galvanic cells in which "activation on demand" via micro fluidic actuation of electrolytes has also been investigated [12-18]. While the proposed cells are not rechargeable, the on-demand concept is attractive, as it overcomes the known degradation over time that most available commercial batteries experience, and provides a disposable device alternative for Power-MEMS.

Results for an aluminum/air semi-fuel cell, formed by layering polymeric and metallic materials, were also previously published by our research group [13]. A thermo-pneumatic actuation mechanism –where, upon heating, a working fluid expands pushing the electrolyte solution– constituting the micro-fluidic actuation, was reported. A second report [14] included a Daniell (Copper-Zinc) electrochemical battery, where each metal electrode compartment contained solutions of its ion salts. The cell activation was proposed via a polyacrylamide swellable polymer that, upon the release of a saline solution, will expand and close the cell circuit. More recently, an electrolytic bubbler was explored to induce the fluidic actuation, to further reduce the activation energy [15]. The addition of hydrogen peroxide to an alkaline electrolyte and other aluminum anode chemistries, coupled either with air or alkali peroxide, conferred higher energetic densities, and were also presented.

Other groups have also reported on fabricating cells whose activation can potentially be achieved by the dispensing of electrolytes. Lee and Lin [16] reported on micro

batteries on a silicon substrate. On top of a nitride passivation layer, alternating PSG (phosphosilicate glass) sacrificial layers and polysilicon layers were patterned in order to form a cavity. A 600x850 um gold electrode was deposited using a lift-off technique. Sulfuric acid and hydrogen peroxide constitute the electrolyte. Sammoura et al [17] developed microbatteries via a two-wafer design. AgCl or CuCl was sputtered to form the cathode. The top wafer is etched using Deep Reactive Ion Etching (DRIE) to provide openings for electrolytes to enter the cell. Magnesium was sputtered onto the bottom side of the wafer to form the anode.

Herein, the fabrication using standard MEMS processes of on-wafer, aluminum anode, galvanic cells is presented. Challenges (adhesion) and resulting process modifications, as well as details about the process conditions and final dimensions of each layer are reported in this paper. Additionally, a preliminary set of performance results that include calculations of energetic content in the cells is presented.

II. OPTIMIZATION OF ALUMINUM UTILIZATION VIA ELECTRODE AREA RATIO

A. *Chemistry*

The oxidation potential of aluminum in alkaline solutions is +2.3 Volts when aluminum changes its oxidation state by three electrons. When these aluminum electrochemical properties are considered along with the low density and atomic weight, theoretical energy densities of aluminum anodes make the use of its chemistries very desirable as an alternative power source (17-24 kJ/gram of aluminum). This fact justifies the intense research activity that has taken place on coupling aluminum with various electrolytes [18-22]. The preferred electrochemical reaction in aluminum anode alkaline cells, in the presence of hydrogen peroxide, $H_2O_{2\,(l)}$ is

$$2Al_{(s)} + 3H_2O_{2(aq)} + 2OH^{-1}{}_{(aq)} \rightarrow 2Al(OH)_4{}^{-1}{}_{(aq)}. \quad (1)$$

In alkaline solutions, in the presence of hydrogen peroxide, competing reactions reduce aluminum anode performance. These reactions, together with over-potential effects (the required voltage to overcome cell internal processes for the charge transfer to occur), reduce the cell energy output well below the theoretical value. One of these competing reactions is known as direct reaction, and takes place when aluminum reacts with hydrogen peroxide to produce aluminum hydroxide. A competing reaction that also produces aluminum hydroxide in addition to hydrogen gas is corrosion.

The desired cathode reaction, which must take place, for eq. 1 to occur is

$$H_2O_{2(aq)} + OH^{-1}{}_{(aq)} + 2\varepsilon \rightarrow 3OH^{-1}{}_{(aq)}. \quad (2)$$

However, hydrogen peroxide decomposition may also occur, where oxygen and water are formed. The release of gases is an issue in these galvanic cells as bubbling interferes with the electrochemical reactions. Aluminum hydroxide scales form around the anode as the alkali hydroxide is depleted, causing interference with eq. 1.

Only in the presence of the hydroxide ion, is the hydrogen peroxide hydrolyzed. This is the initial step in a mechanism in which the overall reaction is eq. 2. Balance of the cathode reaction, as a way to control the hydroxide ions concentration, has been proposed as a viable way to potentially lead to optimum energy output from the galvanic cell. Furthermore, this balancing can be achieved by using a larger cathode area compared to that of the aluminum area [21]. In this paper, a micro fabrication process is proposed to produce cells with varying area ratios, without the need of forming cavities via wafer bonding. Furthermore the cell's testing constitutes a preliminary investigation of the effect of the electrode area ratio on the cells performance.

B. *Mask Design*

This design allows for easy variation of the electrode area ratios via photo-patterning. In this work, the line width, as well as the cell configuration to achieve various platinum-to-aluminum area ratios, have been varied. Testing will determine if the cathode surface with respect to that of the aluminum can potentially benefit the aluminum utilization. In addition, the effect of device geometry is observed. To that end, nine different cell designs were incorporated, consisting of various "mesh" and "ring" configurations. Fig. 1 shows the various designs used in this work. Table 1 provides the

geometric details of each cell. A cross sectional view is shown in section III.

Copies of each of these cell designs were placed at various locations across the wafer to minimize the effects that preferred deposition on certain areas of the wafer (were this to occur in any of the deposition steps) could potentially have on cell performance. The mask was designed in a manner that each 100 mm diameter wafer would host 26 cells.

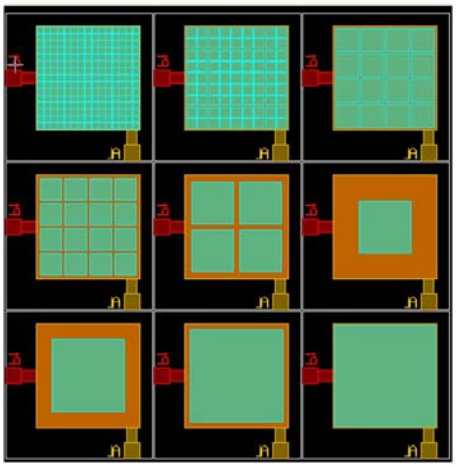

Figure 1. Various cell designs. Note cells 1-3 are on the top row, 4-6 on the middle and 7-9 on the bottom.

Cell ID	Ratio	Line Width (micrometers)
1	8.35	34.5
2	4.26	100
3	4.26	200
4	2.40	320
5	1.78	660
6	0.33	2500
7	0.96	1500
8	4.26	500
9	15.92	150

TABLE I. CELL GEOMETRY

III. MICRO FABRICATION PROCESS DEVELOPMENT

The process begins with <100>, 100mm diameter silicon wafers. The crystal orientation and doping concentration is inconsequential to device operation. The wafers were cleaned with acetone, followed by methanol and deionized water, and spun dry. A low stress, 300 nm thick silicon nitride layer was deposited in a Tystar LPCVD furnace at 835°C for 60 minutes with NH_3 flow rate of 20 scm. Negative photoresist (Futurex NR9-1000PY) was spun onto the wafer at 3000 RPM for 40 seconds, followed by a 150°C pre-exposure bake for 1 minute. Using a mask created to pattern the platinum electrodes and an EVG alignment system, the photoresist was exposed for 11 seconds, followed immediately by a post-exposure bake at 100°C for 1 minute. After allowing the wafer to cool down, the resist was developed in the Futurex RD-6 photoresist developer. After rinsing and spinning dry, the wafer was subjected to heat treatment for another minute at 100°C to drive out any moisture associated with the development process.

In initial attempts, platinum was deposited directly on the silicon nitride passivation layer. Delamination occurred either immediately during the lift-off step or after subsequent processing, regardless of the lift-off technique used (acetone or photoresist remover). Therefore an additional deposition of an adhesion layer was added. Using an AJA model ATA1800 sputtering system, a 10 nm titanium nitride layer was deposited. Deposition time was 3 minutes with RF power set at 360 W, argon flow rate at 29.4 scm, nitrogen flow at 2.6 scm and chamber pressure set at 2 mTorr. This part of the process was modified to test different adhesion layers. Aluminum nitride was deposited with the same power and pressure settings in the AJA sputtering system. Gas flow rates were also 29.4 scm for argon and 2.6 scm for nitrogen. Deposition time was 2 minutes.

In another variation, a 10 nm adhesion layer of silicon was deposited for 2 minutes in an argon plasma using a sputtering system built in-house. The Argon flow rate was 30 scm, RF power was 160W, and chamber pressure was 2 mTorr. Using this same sputtering system, silicon dioxide was deposited. Power and pressure settings were the same as silicon, flow rates were 26 scm for argon and 6 scm for oxygen. Deposition time was 6 minutes. All sputtered depositions were performed at room temperature.

Following the deposition of the adhesion layer, 100 nm of platinum were deposited using the in-house sputtering system for 4 minutes. Flow rate was 30 scm for argon at a pressure of 2mTorr. Lift-off of the platinum was performed using **a** type 1165 photoresist stripper at 80°C. Lift-off times were 15 minutes for the wafers with the silicon and silicon dioxide adhesion layers, 20 minutes for the wafer with the titanium nitride adhesion layer and over 90 minutes for the wafer with aluminum nitride. (Acetone was eventually used in the process after it was ruled out as the cause of delamination.) Upon completion of the lift-off process, the wafer was cleaned with isopropanol and deionized water and spun dry. The wafer with the silicon dioxide adhesion layer was delaminated and did not get processed further.

Next, a 500nm silicon dioxide layer was deposited in a Unaxis 790 PECVD (plasma enhanced chemical vapor deposition).

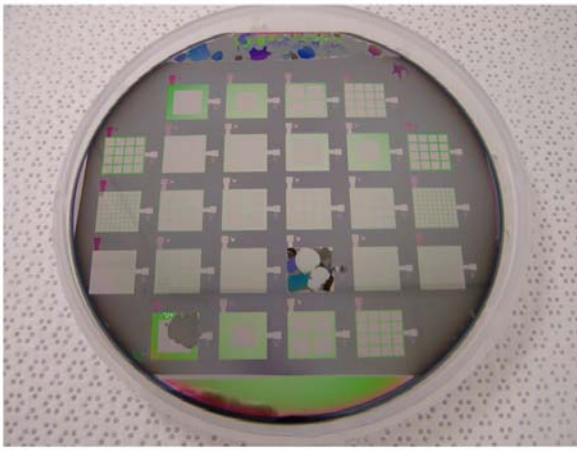

Figure 2. Original process showing patterned oxide where aluminum was expected as well as delaminated platinum

Substrate temperature was 250°C and deposition occurred for 10.5 minutes. The substrate was cooled to 150°C prior to its removal from the chamber.

In the initial attempts, a lift-off process similar to that used for platinum patterning was used for the aluminum deposition. This also resulted in delamination of the aluminum, leaving only the patterned silicon dioxide layer behind (see Fig. 2). An adhesion layer here could potentially affect the operation of the batteries, so the process was updated to etch the aluminum instead.

Using the in-house sputtering system, aluminum was deposited. Again, the argon flow rate was 30 scm. Deposition time was 30 minutes. Aluminum thickness was measured to be 30 nm ± 10% after the etch step using a Tencor profilimeter. Following aluminum deposition, positive photoresist (Shipley 1813) was spun onto the wafer at 3000 RPM for 40 seconds, followed by a 1 minute bake at 90°C. The pattern was aligned and exposed for 1.8 seconds, then developed for 40 seconds in MF 319. The wafer was then rinsed in deionized water and spun dry. The aluminum was etched in aluminum etchant for 8 minutes, under continuous agitation. Upon etch completion, the wafer was rinsed with deionized water and spun dry. The photo resist was then removed using **a** Shipley 1165 photoresist stripper at 80°C for 8 minutes, followed by rinse with isopropanol and deionized water and spun dry. (Note: the process was updated. The photoresist can be removed by spinning at 3000 rpm for 40 seconds with acetone followed by methanol.)

The oxide was etched in a Unaxis 790 RIE system. Etch time was 13 minutes. The platinum electrode acted as an etch stop and the aluminum electrode acted as a mask, preserving the oxide directly under the aluminum electrode. The resulting devices had a total electrode area of 1 cm^2 each. Fig. 3 shows a schematic cross section, as well as a solid model of one of the cells of the device.

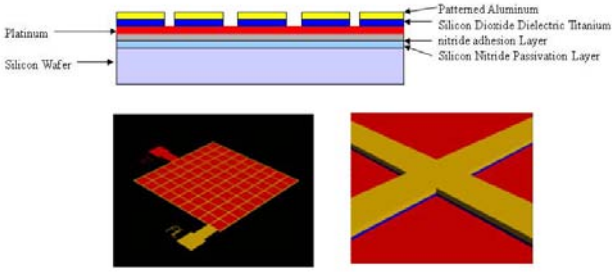

Figure 3. Cross section and solid model of typical cell. Close-up shows the silicon dioxide layer supporting the aluminum grid.

IV. Testing Protocol and Experimental Results

Contact was made to the aluminum and platinum electrodes using a probe station. The initial testing set consisted in subjecting 4.3-Pt:Al area-ratio cells with various ohm loads (no

load, 50 ohms, 100 ohms and 500 ohms). The very small amount of aluminum was expected to react quickly, limiting the life of the cells. The output voltage was monitored by taking data every second with a Fluke 180 logging multimeter. Cells were individually activated using 60 µl of a 1M NaOH solution to which 1 part hydrogen peroxide solution per 9 parts of solution was added.

Further testing was conducted in all of the fabricated cells, where a 100 ohm load was placed across the terminals. As described previously, voltage data as a function of time was recorded after the electrolyte was introduced onto each cell. Instantaneous current and power were calculated from the voltage data and then numerically integrated with respect to time to obtain the current and energy capacity of the cells. Power per gram of aluminum was determined using the area ratios of each cell and the average aluminum thickness of 300 nm.

Cell Performance

Fig. 4 shows the voltage output achieved for replicates of Cell ID #2 (4.3 area ratio) subjected to various loads. Note that as more current is drawn from the cell, the potential decreases, evidence of the existence of overpotentials. The potentials shown in the figure are easily measurable with the multimeter used and these results confirmed that testing can continue for all the cells exclusively with the 100 ohm-load. Fig. 4 also shows various replicates using a 100-ohm-nominal-load which shows the consistency in the obtained data for different cells.

Fig. 5 compares device efficiency for each cell ID with the various adhesion layers. Each set of data shows a trend with the device efficiency being low at low area ratios and becoming asymptotic as the ratio increases. It should be noted that cell ID 8 and 9 (with the ring configuration) did not survive any of the testing (ultra low output) and are not included in these results.

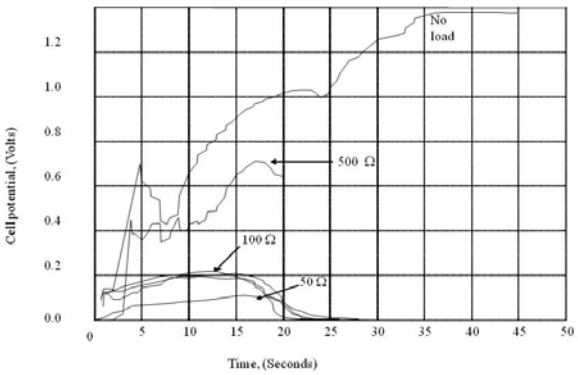

Figure 4. Output of 4.3 area ratio cells under various loads, including multiple replicates under 100 ohm load.

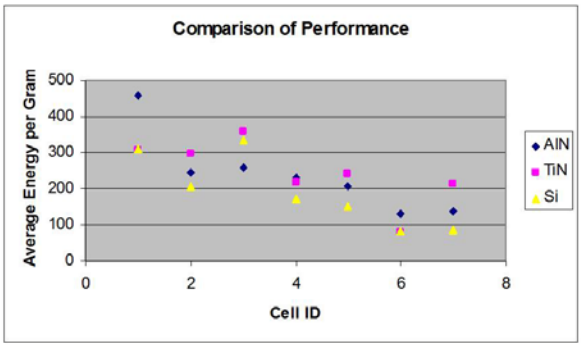

Figure 5. Performance Comparison – Note that cells with higher area ratios (cells ID 1 to 3) tend to have significantly higher energy per gram of Al, regardless of the adhesion material used. Cell geometry data is shown in Table 1. No replicates of cells 8 and 9 produced results.

Note that the various adhesion layers do not have an apparent relevant effect on device performance. This, together with the difficulty of performing lift-off on the wafers with the aluminum nitride adhesion layers led to the decision to proceed using titanium nitride. It is also evident that cells 1 through 3 exhibit significantly higher efficiencies than the other cells.

V. Conclusions and Ongoing Work

The process development for creating aluminum anode, platinum cathode microbatteries on a single passivated silicon wafer is described. The finalized process is

presented in detail, highlighting some difficulties encountered in early attempts. Due to the relative processing ease of titanium nitride, this is the most promising adhesion material. The adhesion material was not expected to have an effect on device performance, and results for all tested cells (for a given device ID) were all within the observed variability for the other cells. All tests indicate that high area ratios of platinum to aluminum produce better device efficiencies, but further experimentation is required to determine if the width of the grid lines affect device efficiency. However, it was shown that a grid-like anode geometry performed significantly better than ring-like geometries.

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Humanware: The Key Element in Educational Technology Projects

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Abstract *— The aim of this paper is to prove and identify Humanware as the key element in any educational technology project, in the different phases of the development IT lifecycle. We emphasize the definition, design and implementation phases where the human factor determines the success or failure of the project. The notable features of Humanware are beyond those of the traditional technology infrastructure where the Hardware and Software are the cornerstones of IT solutions. This paper discusses the social aspects and the democratization of technology thanks to the integration of the human factor and proposes a social technological model focused on the user.*

Keywords*:* Educational, Humanware, Open source, Social Technology.

INTRODUCTION

Educational technology projects have been developed in recent years in the Computer Center department of the University Dr. Jose Matias Delgado (UJMD), El Salvador [1] . Different strategies have focused on the user in order to transform and enhance the student experience as well as the experience of the professor. However, we highlight two new elements for the technology infrastructure, 1) Knowledgeware, defined as the know-how of the user and technician. 2) Humanware, the human factor as the dynamic element that establishes the relationship between humans and technology.

Besides the technological infrastructure, there are many other aspects to consider in our projects. It is important to take into account Open Source alternatives; the advantage relies in the support of the community with a cooperative and collaborative work. It is in this way that we become part of a virtual wide world community. Other aspects to evaluate are the financial and technical possibilities with the purpose to level the impact of the tools and systems.

Higher education tools demand strategies focused on the user, with the Humanware starting the understanding of their needs and creating a bond between the participants in the IT [2] project, sharing their knowledge and socializing technology. Those contributions are reflected in our case study for this paper, Conscius[3].

Conscius has been a rewarding experience for UJMD. The learning platform as a project represents the shift to the socialization of technology. The user is provided with mechanisms of participation that allow them to own the solution. In the context of empowerment of the solution, we highlight its impact within the university community with the indicators of usability and dissemination of the tool.

I. SOCIO-TECHNOLOGICAL MODEL

Prior to developing any educational technological project based on Hardware and Software, the importance of interaction and functionality of the tool must be evaluated by a

[1] www.ujmd.edu.sv/

[2] Information Technology

[3] Conscius, Latin word that means, “Sharing Knowledge”

multidisciplinary team of users. This process begins with the definition of the needs, the solution design and the evaluation of alternatives from the perspective of the user. That is how the Humanware acts into this Social - Technological model. (Fig 1). This represents a challenge for IT management; the human factor is incorporated into the project phases in such a way that Human Interaction with technology built a new model and introduced a change into the educational culture.

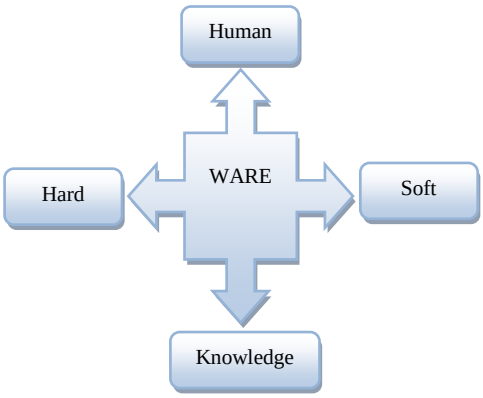

Figure 1. Social - Technological Model

Humanware as a technological concept has not been discussed or studied as the Hardware and Software have [1]. The integration of the human factor may be able to explain the meaning of this interaction and implication in projects oriented towards higher education, where we have a variety of user profiles such as technicians, academics and researchers. The users assumed their role in the process of contribution of knowledge from the social constructive approach[4] of learning.

Human contribution in technology promotes modifications in IT choices and criteria like usability and feasibility. The management and administration of projects are sensible to the human factor, where relationship and interaction with technology generates new actions context and new horizons. Under this context socialization of technology is established, where the relation, collaboration and cooperation of the individuals are reflected in the human factor.

[4] Theory studied by Lev Semyónovich Vigótsky

Based on this social – technological model, the UJMD´s experience creates the shift from traditional IT projects to projects focused on the user, highlighting the aperture of changes and innovation from higher authorities of the university by supporting and integrating the human factor in its technological and educational infrastructure.

II. HUMANWARE CONTRIBUTIONS

The integration of Humanware in the model and in the social technological infrastructure brings with it new concepts and challenges. We identify the presence of multidisciplinary teams in the phases of the project as well as the socialization and democratization of the technology.

The socialization starts with the following variables in technology:

- Project management areas.
- Human – Computer Interaction
- Software lifecycle intervention.

These aspects respond to the social approach and highlight several indicators: 1) Design, 2) Interaction, 3) Usability, 4) Adaptability and 5) Security criteria. They are considered for project development and implementation. The success of the model relies in the democratic process of acceptance by the user community extended by a multiplier effect.

A. Human Know-how

The value and the major contribution from the human factor is knowledge. The know-how belongs to the user and that enriches the logic of the machine. We can call it Knowledgeware, one of the fundamental components in the social – technological model.

There is no doubt that Humanware permeates innovation in the traditional infrastructure and attempts to improve software engineering and hardware capabilities. (Fig. 2).

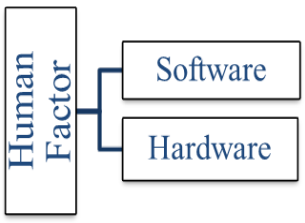

Figure 2. Human Factor relationship

B. Empowering the user

Own the solution, empower the users and respond to their needs. The process begins with brainstorming meetings in order to build the objectives, scope and functionality of the tool. Once that the goal is clear we start to evaluate software alternatives based on the needs and particular user profiles, in our higher educational context with roles as student, teacher and technicians taken into account for the final solution.

As we can see, technology is sensible to the human element, and a tool's performance depends on the level of compromise from the IT developer and the user.

III. CONSCIUS, SHARING THE KNOWLEDGE

In educational projects, the development of platforms and eLearning environments demands the introduction of new information and communications techniques, backed by the theory of social constructive learning.

The educational project catalog from UJMD, includes a variety of initiatives oriented to socialize technology and share knowledge among the community. The project Conscious was created under this philosophy in order to provide an eLearning platform with the following characteristics: an Open Source solution supported by an eLearning worldwide community; a low cost financial alternative which permits the reorientation of investment in the human resource for their training and service availability.

Prior to Conscius, UJMD was under the owner platform Learning Space, and it can be mentioned that this tool was implanted as a necessity of the institution for improving the space of learning oriented to all the resources and the investment of hardware and software. The proprietary character of the tool and higher costs of maintenance were the indicators that propelled an attitude of change for IT projects in the educational context. However, one of the reasons for this major incidence was the low adoption within the teacher community.

Conscius made an impact in the history of modernization on educational technological projects UJMD; the human factor was involved in the different project phases. Fig. 3. The aperture to innovation from the university rectory was a determining element for a series of initiatives focused in the human factor as well the initiative from the Computer Center department.

Figure 3. Conscius phases

A. Conscius background

The Learning Space platform was implemented in 2000 however, it was not until 2002 when two faculties, Health and Economics, started to use the tool as an educational web base supporting resource. The adoption impact was very discrete but with this initiative an innovator and challenger project started to emerge.

In 2004 Conscius, Fig 4, was launched as the eLearning platform based on Moodle [5], well known as a learning management system. This tool helped teachers to upload educational content in any digital format, enhance communication, facilitate cooperation and create a collaborative environment.

[5] http://moodle.org/

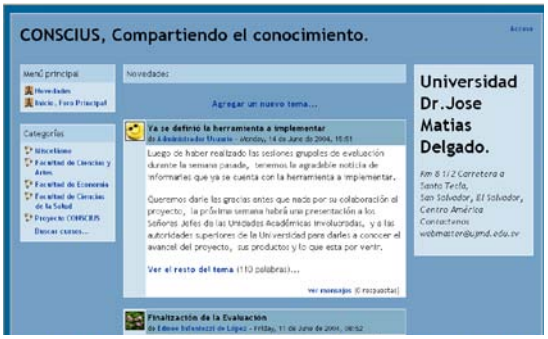

Fig. 4. http://www.conscius.ujmd.edu.sv/login/index.php Conscius platform 2004

TABLE I. COMPARATIVE INDICATORS 2004

Indicators	Learning Space	Moodle
Courses	45	149
Students	**545**	**2137**
Teachers	52	81
investment	$ 200,100	$6,800

Conscius has incorporated the human factor since the very early project phases. Some indicators, Table I, show the user impact in acceptance and use for their courses. Their approval was apparent for two reasons: 1) availability of learning platform licenses and 2) The easy use of the tool.

There is no doubt that including a multidisciplinary team brings benefits, highlighting the participation and collaboration of the users from their profiles and know-how in the teaching - learning process. User participation was delivered in workshops that identified and defined their needs according their profiles. Learning platforms were evaluated establishing the criteria for the following aspects:

- Design and Interaction.
- Navigation.
- Curricular adaptation.
- Security.
- Availability
- Flexibility in the edition of contents.

The promotion process and dissemination of the tool was provided by the teachers involved in the evaluation and use of Conscius, acting as knowledge channels of transference. Currently, Conscius is the Learning platform use by UJMD, with 6500 users annually and an estimated 330 teachers using the tool for their different courses.

B. After Conscius

After Conscius's release, Conscius Satellite entered our projects, Fig. 5. This project was oriented to deliver Conscius's content offline. This was another Open Source solution where financial and technical advantages are taken into account. However, the impact was very subtle and it didn't reach the previous success because the human factor was not a priority in the definition and evaluation of the tool. Humanware's absence resulted in low levels of acceptance of the tool. Previous experiences discussed in the paper affirm the value and contribution of human factors in implementing solutions, and determining the success of the tools.

Figure 5.Conscius Satellite

Other kinds of projects have been implemented in UJMD Computer Center, including: university entrepreneurship; open source clubs and an Educational Informatics Network for future research lines. They all have in common the main goal, involving the human factor in technology and sharing knowledge.

IV. CONCLUSIONS

Each of the initiatives mentioned in the paper take into consideration technological, financial and human factors in order to provide real solutions for the user, in our case the student and teacher members of the UJMD community. Our audience defines the type of interaction and provides a profile classification.

There are three key elements responsible for Conscius' success:

1) Acceptance of the change of attitude towards open source alternatives.
2) Investment in Humanware.
3) The incorporation of the social–technological model, focusing on the user perspective.

Based on our experience, the support and determination from higher authorities in Educational Technological Projects are the beginning of this change of attitude and wide deployment of IT initiatives that improve the student achievement and enhance the teaching–learning experience for everyone.

We emphasize as a priority the Humanware in any Educational Technological project; we have learned the importance of the multidisciplinary team and the establishment of a collaborative network among the users. In the future we expect to create a wide Educational Information Network, with the primary goal of sharing knowledge.

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Intelligent Authoring Tools for Digital 3D Interactive Contents Towards a Knowledge Industry in Colombia

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Abstract *— The Colombian Government has recently launched an ambitious ICT plan of USD 3000,000,000 for the next 4 years to achieve social and technological insertion of this country in the Knowledge Society. A major concern is that the human resources and intellectual capital at Higher Education needed to meet the challenges posed for said Colombian Strategy are scarce.*

Our work discusses the following major issues:

- *Improving the productivity of students and teachers through extended learning and lecturing with intelligent tools and a new pedagogic model involved.*
- *Forming Author Lecturers for creating digital content to produce 3D interactive self-learning educational contents using augmented and virtual reality, so that students may have experience with applications in Virtual Simulation.*
- *Editing & creative authoring of Interactive Living Books.*
- *Permanent upgrading of new interactive learning & self educational devices/material.*
- *Creating and maintaining new 3-D interactive bibliographical data bases with stand-alone, on-line and mobile file applications.*

The final purposes in terms of expected results are the following:

- *Creating an Industry for digital 3D Interactive Contents in Colombia's Knowledge Society with state-of-the-art technology.*
- *Creating various specialized teams of authors, producers and tutors of simulation systems and their applications.*
- *Creating an International Certification Unit in the subjects mentioned above within our Institution.*

Several research projects are underway in the FESSANJOSE- related to:

- *Intelligent System Tools for Undergraduate and Graduate Students & Teachers: iCOACH [3].*
- *Cognitive Managers: Competence and Knowledge Management and Managers.*
- *Models: Analytic Tools for Academic and Management Governance; Tools for Future Strategic Analysis [5] [7].*
- *ICT Powered Education for Industrial Productivity.*

The Government of Colombia has been working to increase the coverage in higher education by enacting the 1188 Law of Education of 2008, recently regulated by the Decree 3495 that mainly promotes quality conditions and standards to strengthen the national quality system in Superior Education and to introduce the possibility of democratizing knowledge, enabling the opening of education by Propaedeutic Cycles, i. e. Professional Technician, Technology, and University degrees on engineering education.

The skills and professional profiles of each Propaedeutic cycle are described within our curricular coherence matrix.

The Colombian ICT National Law 1341 of 2009 was enacted to narrow the gap between Colombian students and these new

technologies; in addition, it evolves towards the latest advancements in media and communication technology, including those developments that allow the Knowledge and Software Industry to accomplish improved competitiveness with new technological solutions, which in turn will facilitate Colombian social and economic emergence through the various applications enabled by this new knowledge industry.

A brief discussion is given to conceptualize this new industry through given inputs and byproducts, production functions, intellectual capital formation, intellectual assets, artifacts vs. mental-facts and many others. In this sense FESSANJOSE leads several research projects aimed to build intelligent authoring tools and re-qualification of teachers and lecturers at work in order to generate new knowledge and digital contents for ICT/Virtual Education.

Initially, we are planning to train around 600,000 teachers and lecturers, including the re-qualified workforce, within the next 4 years. An important item of these figures will be the number of new permanent jobs created: at least 100,000.

***Keywords**:* Authoring tools, Augmented reality, Intelligent knowledge based systems, ICT, Hypermedia, Virtual reality.

I. RATIONALE

A. Background

Tertiary student desertion is a nationwide problem in Colombia, critically impacting culture, economy and society in general. Several IES (Superior Education Institutions) have performed studies pointing out the prevalence and recurrence of this problem. Another problem is the academic governability of the IES Institutions which imply additional demands for their management, including financial sustainability.

One answer that addresses all these problems is our research Project: intelligent virtual systems with mathematical and computational analysis capabilities. It includes the design and implementation of the iCOACH model, a knowledge-based intelligence tool, presented as a high computing instrument designed to follow up with each student throughout the academic curricula in the relevant engineering school at the FESSANJOSE.

The software architecture has 3 main parts: an Edumatic Builder (a tool for improving Professor productivity), the Student Model (a personal model in which all competencies acquired are registered historically), and lastly: a knowledge base for concept verification and related items.

Also, a Knowledge-based system model to face the new methodological strategy on Higher Education for Colombia is presented: the Propaedeutic Cycles.

First, with a set of analytical and mathematical tools that allows management quantification and curricular knowledge: the FESSJ-PROP model, which is a structural system for analyzing and structuring cohesion and consistency among these cycles. Among the purposes and scope of the linear model of consistency in curricular knowledge is the simplified understanding of the methodological strategy for propaedeutic cycles and college resource optimization. Several Leontief Model extensibilities by Linear Programming and Input-Output, which analyzes dropout complexity, are included. The objective functions have 3 student levels: Deserters, In Recuperation, and Good Performance.

The latter have approached the problem by migrating from the Inter-industrial Economy Model to the new Knowledge Economy Model, by re-contextualizing the W. LEONTIEF Model from the Industrial Society to the Knowledge Society, updating it by introducing a Process Engineering model, an Artificial and Computational Intelligence

model, and a Knowledge Management and Engineering model [5] [7].

B. Specific Objectives

The aforementioned tools are required to improve the cognitive productivity of students who are exposed to a coaching system in order to strengthen their learning.

For Teachers these intelligent tools involve a pedagogic model to improve the evaluation content expertise with new functionalities.

Another goal is forming Author Lecturers capable of Creating Digital Content to produce 3D Interactive Self-learning Educational tools using Augmented and Virtual Reality, so that Students may have experience with applications that include several modern techniques such as interactive virtual simulation and immersive worlds. They also Include Creators & Authors of Interactive Living Books.

C. Final Objective

The new ICT aggressive plan of Colombia mentioned above implies a social and technological agreement of the National Administration to insert our country in the Knowledge Society. These national policies present a new challenge: creating a new economy based on knowledge and information.

Our tools aim to create a Knowledge Industry based on digital 3D Interactive Contents for the Colombian Society of the Third Millennium. In this country, the National Education Ministry has trained 50,000 teachers on general tools for virtual education (e.g. Moodle) in 3 years. With our tools we expect to train 600,000 teachers at all education levels and update their job qualifications for the new economy. A great number of these jobs (100,000) will be both new and permanent. These people will build a specialized critical mass of authors and producers of simulation systems and applications in order to strengthen the knowledge industry. *Pari passu* is the creation of an International Certification Unit in the above mentioned subjects within our Institution, FESSANJOSE.

II. DESCRIPTION

A. Towards a Knowledge Industry in Colombia

Clearly, this industry is a mind-intensive work in which labor is an additional component to the artifacts: mental tasks to be completed by knowledge workers. Also the capital has an additional dimension within intellectual and asset capital. Knowledge has its own life cycle: acquisition, storage, dissemination, and application. This cycle is a sequence of intellectual tasks by which knowledge workers build their unique, competitive advantage for social and environmental benefit. It also comprises a range of strategies and practices used in an organization to identify, generate, display, represent, distribute, and enable the adoption of insights and experiences (knowledge).

An economy of knowledge focused on the production and management of knowledge in the frame of economic constraints is a knowledge-based economy. This definition, the more frequently used, refers to the use of knowledge technologies (such as knowledge engineering and knowledge management) to produce economic benefits as well as job generation.

Various observers describe today's global economy as one in transition to a "knowledge economy", as an extension to a "postindustrial economy". Such a transition requires rewriting the rules and practices that determined success in the industrial economy.

This new economy is an interconnected, globalized one where knowledge resources such as professional competencies and expertise are as critical as other economic resources. According to the analysts of the "knowledge economy", these rules need to be rewritten at all levels: from firms and industries to public and politics, as well as ICT & knowledge-related topics.

In a knowledge economy society, knowledge is an input/output product (regarding Leontief), while in Knowledge Engineering (KE), knowledge is a resource/tool. This difference is not yet well distinguished in the subject matter literature. They are strongly interdisciplinary, involving economists, computer scientists, software engineers, mathematicians, chemists and physicists, as well as “cognitivists”, psychologists and sociologists. KE is an engineering discipline that involves integrating knowledge into computer systems (expert systems) in order to solve complex problems normally requiring a high level of competences, know-how and expertise. At present, it refers to the building, maintaining and development of knowledge-based systems. It has a great deal in common with software engineering, and it is used in many computer science domains such as artificial and computational intelligence including knowledge-based databases, Business Intelligence, knowledge based expert systems, decision support technology and many other IKB systems. Knowledge engineering is also related to mathematical logic, and is deeply involved in cognitive science and socio-cognitive engineering where knowledge is produced by socio-cognitive aggregates (mainly humans) and is structured according to our understanding of how human reasoning and logic works.

The new knowledge industry may create new jobs such as Knowledge Engineers, Knowledge software Architects, Knowledge base Administrators, Knowledge requirements Analysts, Knowledge Authoring teachers and lecturers, Testing Knowledge bases Technologist, Data and Knowledge Stewards, Knowledge technicians Architects, Quality Knowledge Assurance Technologists, Technologist of Knowledge Governance and many others.

B. Pedagogic Model Description

Our Instructional System distinguishes three stages in distance learning, which suggest strategies to incorporate into a tutorial. The first refers to pre-seasonal activities in which motivational efforts are needed to encourage the student to achieve some concrete goals in terms of certain cognitive skills, e. g., troubleshooting. This should be reflected in the definition of goals and objectives throughout the material. A second instance refers to activities in which the author provokes reflection on knowledge, active experimentation to test knowledge, and others. The third stage is the Post-session in which feedback should be promoted and strengthened by evaluative questions and summarizing which allow the viewing, distant learner to become cognitive through achievable goals at the end of the course, while causing him to anticipate the knowledge to be acquired in the next phase.

Another requirement is related to advanced organizers as a presentation of introductory content, characterized by being perfectly clear, stable, relevant, and inclusive of the content being taught. Their main function is to establish a bridge between what students already know and what they need to know before actually learning new content. A good advanced organizer is able to integrate and to interrelate the material. There will be a summary or overview, as presented in the books, as they are often proposed at the same level of abstraction and generalization as subsequent learning material. Advanced organizers shall be highly abstract, general and inclusive in order to be effective.

The student model keeps a diary iCOACH of the skills each student has acquired allowing test customization, as well as assessment of prior experience and, if possible, projection of the motivational aspects of each student.

III. REQUIRED FUNCIONALITIES

A. Student and Teacher Productivity

Developing learning content involves at least 2 aspects that make the process cumbersome for the authors. The first is the variety of competencies, skills, abilities, capabilities, and expertise to be developed by the students. The second relates to the variety of subjects and their related cycles for updating. Authors have to create units of learning for the student, scripts for the classes, and tests for concept verification, practical sessions, interactive 3D simulations, hypermedia material, problem sets, learning pills (flashcards), and many others. Consequently, their production becomes quite complex. The above are some of the reasons to develop intelligent tools to face these complexities Another reason is to facilitate the training of thousands of authoring teachers and the creation of positions for the new knowledge industry, as mentioned above.

B. Authoring System Architecture.

Our architecture has 2 main components:

One component is related to the models. At least three models are involved: The Student Model, The Teacher Model (which implies his/her cognitive style) and Syllabus and Planning Model (rules, restrictions or sequencing strategies, courses, modules, presentations)

- The second component is a Virtual Tutor, a sophisticated set of instructional primitives and multiple tutoring strategies.

C. Functionalities

The following list enumerates several prototype functions, most of which are partially implemented with our prototypes: the management of at least 30 types of item formats, including the following:

- Multiple choices with single answer or Multiple answers, scoring of all response options to set the number of options that must be taken in response.
- Rank in order of response options scoring matrix to assess potential order.
- Pairing or correspondence
- Fill in the blanks: one or multiple
- Response Test
- Oral Response
- Question and numerical answer
- True and False

D. CAPABILITIES TO RESPOND:

- Drag and Drop
- Display with explanations
- Place hot spot
- Selection of options from a drop-down list
- Features to produce items
- Inserting images, audio, video
- Inserting hypermedia materials.

E. TESTS AND ITEMS ADMINISTRATOR

- Storage and management of questions on local and remote repositories
- Organization of items by "issues" with classification levels and sublevels
- Wizard building items
- Integration of multimedia elements (full audio, full video) and repository
- Integration of graphics (GIF, JPEG, PNG, WMF, BMP), unlimited repository of these elements
- Schema Definition scoring and weighting of items in the tests as defined by structures and needs

- Import/Export questions according to international standards
- Collaboration with multiple authors
- Workflow Settings for the development and implementation of test questions
- Implementation of roles or user profiles and assigning permissions to access or security functions and levels
- Last modified audit.

F. BUILDING TESTS

- Management of test structures as needed
- Organizing questions into exams (based on predefined structures)
- Intentional or random selection of questions for meta-tags or specific subjects
- Defining representation of questions in the test structure (predefined, random or branched) and management of pre-defined or random response options
- Multiple forms of representation of questions (one by one in list, block)
- Response time limit per item or test block.
- Control of the evaluated time (display or hide)
- Different forms of evaluated test representation: browser-based online, CD, print, PDA, Cellular
- Delivery assurance levels by browser
- Customizing the test by inserting participant name, date and time
- Customizing the rendering format (questions and tests)
- Customizing the test at the end of page.

G. KNOWLEDGE BASE CONTENTS

- Options to cut, copy and paste into the handling of questions, assessments and resource files
- Modification of representation by more than one author, and author control
- Multiple authors simultaneously developing and publishing content in the repository
- Linking E-learning/M-learning contents and test questions.

H. SECURITY SYSTEM

- Definition of roles and permissions for administrator and author levels; Delimitation of logins by IP; Folder Access Control
- Security control to protect tests from being copied, printed or shared on the computer where the test is developed.

IV. CONCLUSIONS

A. WORK IN PROGRESS

Several projects inside our research efforts are underway. The new academic program on systems engineering with the methodological strategy on Virtual Education is in progress. To date, it is the first program structured by propaedeutic cycles in this country [8]. It required working with other fields related firstly with the student cognitive style investigation and secondly with his/her characterization and features. Felder Test and the EEPA Test were both applied. The investigations resulted on four bipolar scales: Active - Reflective, Sensing - Intuitive, Visual - Verbal and Sequential - Global. Moreover, the EEPA Test is an assessment based on problem solving, producing results on four learning styles: diverging, converging, assimilated and accommodated.

The purpose of the classification was to characterize the socio-educational profile of students in the engineering systems academic program, which enabled us to understand the social and academic status that may impact their performance. This facilitated the design of virtual program contents for the new Systems Engineering Virtual Program by Propaedeutic Cycles.

B. FUTURE RESEARCH WORK

As part of the European Community Convocation (Sala 3D), links and partnerships should be identified and established to produce knowledge. Among the highlights of future projects:

- Creation of a Centre of Excellence for Teacher Training-authors of thematic content, evaluative, digital (Multimedia and Virtual Reality extended), supported by three-dimensional interactive simulation instruments.
- Fundraising for professional software development is imperative. Development complies with international standards to build and consolidate the intelligent tools matrix analysis of curricular coherence, so widespread and friendly efficient management involves Curriculum for each propaedeutic cycle. The above mentioned instruments aid competence management, with different granularity.

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A Practical Approach to Education of Embedded Systems Engineering

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Abstract *— It is very common to see that in almost every daily routine, digital electronic devices provide vast comfort and flexibility for consumers. Companies designing and manufacturing these devices use advanced hardware and software tools. Engineering graduates sometimes have difficulty securing an entry-level industry job since there are major differences between what they have learned in school and the latest technological development tools used in the industry. In this paper, a state of the art embedded systems laboratory course is introduced. This lab course helps students with the experience of designing and implementing applications in embedded systems by using modern hardware and software development tools. It aims to teach theoretical and practical, organizational and architectural concepts regarding microprocessors via advanced engineering projects. The evaluation of the course indicates that most of the objectives have been achieved.*

Keywords*:* Electrical Engineering Laboratory, Embedded Systems Design, Engineering Workforce Development Introduction Microprocessors Based Systems.

Digital electronics devices have been a critical part of human lives over the last two decades. It is easy to see that these devices are being heavily used in every environment where humans interact such as medical, security, and communications to name a few. Therefore, the design and enhancement of these devices are crucial to fulfill the future consumer requirements. In this regard, electronics device manufacturers have to maintain the quality of their engineer recruitments in such a way that not only responds to the consumer needs but also creates new developments and innovations. To be able to do that, the educational methodology of future engineers at universities plays a core role in preparing their students for jobs in the industry by introducing and teaching current technological advancements in the context of embedded systems hardware and software implementations.

The Department of Electrical Engineering at the University of South Florida (USF) has seen this necessity and has consequently developed a state of the art embedded systems laboratory course that enables its students to interact with the latest technological development tools, and provides creative environments to design their own projects. The lab aims to teach organizational and architectural concepts of microprocessors via introducing advanced engineering projects which help students to clarify the idea of how to integrate both hardware and software embedded systems skills.

For the required hardware and software development tools, the department collaborated with Freescale, one of the leading global semiconductor companies, to establish the laboratory course. The Tower System [1], which is one of the recent Freescale products, was chosen as the hardware development environment. CodeWarrior was also chosen as a computer aided design (CAD) tool for implementing software solutions. These tools are the integral parts of the laboratory setup. Equipped laboratory benches are very flexible, and allow students to conduct lab experiments and to create their own projects consisting of hardware and software modules

This work was supported by Freescale Semiconductor, Inc.

supported by the Tower System. These modules ranges from general purpose input and output (GPIO) units, analog to digital converters (ADCs), interrupt service mechanisms (ISRs), timers, serial communication interface units (SCIs), Ethernet, sensor managements (potentiometer, accelerometer) to some other peripheral units such as memory units, etc. which are common among most microprocessors.

In this paper, an overview of the philosophical approaches on how to manage and create advanced engineering projects is described in detail. Evaluation results show how this new lab course can extend students' engineering visions and support their senior-year projects.

I. CONTENT OF THE LABORATORY COURSE

The lab course relies mostly on the introduction of hardware structures and the explanation of software implementations. Besides these clarifications, the general concepts of digital systems and microprocessors are also given at the beginning of the semester. Some important concepts of architectural organizations of microprocessors are also explained in detail to help students visualize how microprocessors are designed and how they operate.

Introduction to embedded systems programming is also presented to students in the beginning of the lab course. Since today's microprocessors are constructed with very powerful hardware units, the software programming of these devices has become more challenging. One of the important byproducts of the developed lab course is to let students learn C programming language with real time hardware applications. The development board has a real time operating system (RTOS) called MQX to run given applications. This sophisticated RTOS has numerous libraries to enable proper functionality operation. In this regard, the tutorial of the C programming is given in the light of introduction to MQX libraries and its functionality. Students are exposed in order to grasp software mentality and then expected to make reasonable connections between software and hardware organizations in such examples as how a hardware unit is represented as a structure in software manner.

Embedded systems programming started with the implementation of applications written in Assembly language, and then continued with the coexistence of Assembly and the C programming. Especially after the Internet processors came out, software implementation of embedded systems has become more modular and increasingly complex. This programming technique called advanced C programming is the primary method of software implementation in the lab course. All lab experiments are based on this technique with MQX functionality. However, the first experiment is presented to students in three different programming language formats, which are Assembly, Basic C and Advanced C respectively. The first experiment is designed to show how embedded systems programming has evolved in terms of design flexibility and modularity.

A threefold method is applied for the instruction of each lab experiment. The content of lab experiments are based on this method and each experiment step is documented in the lab manual [2]. First, a new hardware unit is introduced to students. The corresponding hardware structure, its register organization and pin mapping are explained in detail. Then, an application idea is put forward for the students' consideration. Over a selected hardware unit, the application is put into effect. During this process, the instructions that must be followed during the hardware implementation are explained, and then related pin assignments and other external connections are demonstrated Secondly, intellectual software organization is as depicted in MQX libraries representing the related hardware unit is shown. The essential variable declaration, functions and programming method are described. Lastly, the software implementation of the lab experiment on The Tower System is carried out in light of objectives stated in the lab manuals.

From the explanations of the issues discussed above, as illustrated in Fig.1, the ultimate objective of this lab course is to let students use hardware and software development tools effectively to create state-of-the-art engineering applications.

II. COURSE STRUCTURE AND LABORATORY EXPERIMENTS

The course is based on the successful completion of all the mandatory experiments and a design project. A few assignments as well as pop-quizzes throughout the semester are given. Moreover, a few optional advanced experiments are done if there is no time limitation. All mandatory experiments, assignments and a design project are carried out by lab teams, which are set to include no more than three students; however, writing a report for each application is an individual effort.

The lab course is offered to senior year students. C for Engineers and Logic Design are chosen as prerequisite courses.

For lab experiments, TWR-MCF51CN-KIT is used as the hardware development board. Lab experiments are designed to employ an on-board microprocessor, MCF51CN128, and external hardware extensions which are four LEDs, two push buttons, two DIP switches, a potentiometer, an accelerometer, a RS232 port, and an Ethernet port.

A brief description of mandatory experiments is given below:

1) Comparison of Assembly, Basic C and Advanced C with General Purpose Input Output (GPIO)

The objective of this experiment is to create an application which basically programs on-board LEDs to blink within specific time intervals, and to write related source code in Assembly, Basic C and Advanced C. This is a first experiment, to show how embedded systems programming techniques have evolved in time.

2) Exploring Real Time Operating System (RTOS), Freescale MQX, and more GPIO utilization

Starting from this experiment, MQX and its functionality will be further emphasized, and used for software implementations. The usage of the GPIO unit is explored in depth throughout this experiment, especially by focusing on its different data direction selections (Input/Output). The planned application for this experiment is that by using either onboard switches or buttons, external user interventions are perceived, and LEDs start to blink in different formats.

3) More student involvement into driving GPIO

This experiment aims to increase student excitement by letting them create their own user-defined functions to control MQX and GPIO unit. As a model application, a four bit binary counter is implemented by using LEDs and push buttons. The application includes using push buttons to increase or decrease the counter by one, and showing it over LEDs.

4) Driving an Analog to Digital Converter (ADC) device, Potentiometer

The experiment starts with a brief explanation of the principle of analog-to-digital conversion method and sampling theorem. Some important design parameters such as resolution, sampling rate, and quantization error are explained in detail. The desired application of this experiment is to read analog inputs from on-board potentiometer in a digital format, and then depending on its rotation level (magnitude of readings) is to set the number of alight LEDs.

5) More ADC utilization, Accelerometer

The objective of this experiment is the implementation of a motion detection algorithm on the development board. On-board accelerometer is used for this purpose. Therefore, besides similar instructions given for reading analog channels in the previous experiment, the hardware structure and working principle of an accelerometer is exposed to students.

6) Driving a Serial Communication Interface (SCI) device, RS-232 port

This experiment establishes a connection between the development board and PC over a serial communication interface. Characters typed through the keyboard are sent to the board, and bounced back to the PC. All transactions can be visible over HyperTerminal.

7) Setting up Timers

The objective is to set up two different timers to trigger two different user-defined functions. Each timer runs for a second, and then sleeps for a second. One of timers is forced to start running a second before the other starts. Therefore, two user-

defined functions are triggered a second after another. User-defined functions are responsible for turning LEDs on or off. As a result, LEDs blink constantly every second.

8) Understanding of Interrupts

Multi-tasking is one of the important features that are brought by MQX. Until this experiment, software implementations have been based on polling methodology when needed. Triggering interrupts are not used for prompting different tasks. In this experiment, a user-defined interrupt service routine (ISR) is designed to take the place of a timer interrupt service module. The new ISR basically has a static counter value, and whenever called, it increments the counter by one. The objective of this experiment is after setting the new ISR, to wait for a while and then to check how many interrupts has occurred.

After the 3rd, 5th and 8th experiments, assignments are given to students. They have to create any application which consists of topics that been covered up to that time.

A brief description of optional (more advanced) experiments is given below:

9) Trivial File System (TFS) and Memory Management

This experiment intends to create a file directory in the flash memory, and to put some text files in this directory.

10) Real Time TCP/IP Communication Suite (RTCS) and Telnet

This experiment is prepared to show a piece of advanced application which shows how far embedded system technology can reach nowadays. A communication is established between a microprocessor and PC via the Internet. In able to do that, some important steps are explained in advance such as creating RTCS, setting local IP addresses, obtaining Ethernet MAC addresses, initializing the Ethernet device and binding IP addresses to the network over Telnet-ported sockets. On the other hand, shell console programming is used to recognize user-defined commands and execute them over Telnet connection. User-defined commands are chosen by turning on/off LEDs, reading a file in memory, and querying a counter for getting the number interrupt occurrences for a given time duration.

11) Web Server, Dynamic Course Web Page Design

The experiment includes creating a HTTP server and running a dynamic web page in the microprocessor. The web page shows the active status of LEDs, push buttons and potentiometer, and updates these statuses dynamically whenever any of them changes physically.

Pop-quizzes are usually given a week after a new hardware device has been successfully introduced.

For the final project, lab teams have to create a unique project idea which shows their interest in embedded systems.

TABLE I. LAB COURSE PLAN

Weeks	Labs	Topics
#1	Intro to Digital Systems	
#2	Intro to C Programming	
#3	Week #2 Cont.	
#4	Intro to The Tower System	
#5	Lab #1	Assembly Language (GPIO)
#6	Lab #1 Cont.	Basic C & Advanced C (GPIO)
#7	Lab #2	GPIO (Gen. Purpose Input/Output)
#8	Lab #3	GPIO
#9	Student Exercise #1	GPIO
#10	Lab #4	ADC (Analog to Digital Conv.)
#11	Lab #5	ADC
#12	Student Exercise #2	ADC
#13	Lab #6	SCI (Serial Comm.)
#14	Lab #7	Timers
#15	Lab #8	Interrupts
#16	FINAL PROJECT DUE	

III. APPLIED METHODOLOGY

This lab course has been offered for the last three semesters. Due to time limitation during the semester and overall student assessment, the context of the lab course has been shortened to achieve proper and effective understanding of the course by students. Table I shows the course plan followed during the semester. As shown above, the lab course is student-oriented. The advanced labs are omitted, and they are reserved as an optional course of study for senior year project topics.

Covered topics include the most important sections in embedded systems. Students are exposed to the learning process of embedded

systems from scratch for them to become capable of creating advanced projects.

The weeks where student exercises are held are reserved for creating an original project proposed by students instantly. The intention is to show how a project idea is turned into a real design and its implementation.

IV. Evaluation of the Course

The evaluation of the Embedded Systems Laboratory course is made with the outcomes of questionnaires asked to students. The questions are prepared to collect students' opinions and experiences after taking the lab course. The evaluation results stand as a key point for the future improvement of the lab course to respond to students' needs and meet the desired objectives.

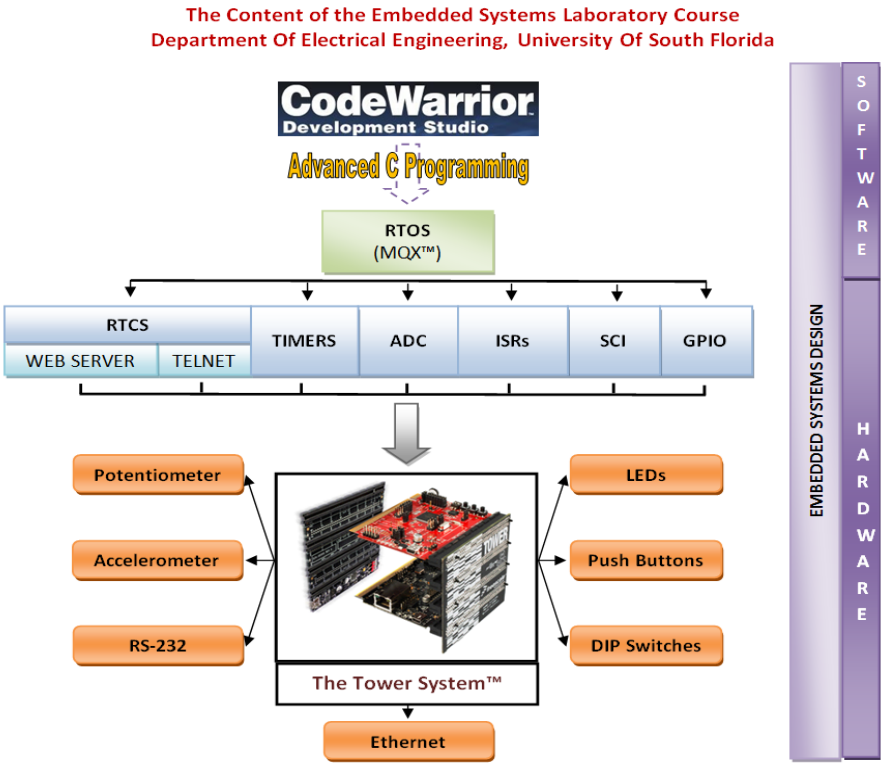

Figure 1. Content of the Lab Course

First of all, students feel excitement to create interesting projects. They find the lab course very interesting thanks to seeing some examples of state of the art applications in embedded systems design. They state that their interest into engineering and development of the technology has arisen after taking this lab course. According to their opinions, the way that they look at the consumer electronics devices, such as cell phones and mp3 players, have been evolving from the consumer perspective to the engineer perspective, especially thinking of how these devices are designed as a combination of both hardware and software.

Moreover, even if they have difficulty understanding and writing C programming code for applications, they agree with the idea that Advanced C supported with a rich set of MQX functionalities is a powerful tool for embedded systems applications. They confirm that learning a high level language is very helpful to design and improve the engineering project with the supporting of real implementations and simulations.

Another important issue which is pointed out by students is that the lab course helps them ~~to~~ understand organizational and architectural concepts of microprocessors better, and improves their knowledge of using hardware and software development tools in embedded systems design. Students think that this lab course is where theory meets practical engineering. The lab course covers enough theoretical information ranging from digital communication to logical design, from networks to circuit organizations concisely to be implemented practically in the platform of embedded systems.

Furthermore, students find the lab manual very useful since it walks them through the whole process step-by-step and helps them understand what is being done.

On the other hand, some students complain about the workload for writing reports after each lab or assignment, and find the time duration to submit them limited. Besides that, a few students criticize C programming requirements for the lab course. They believe it is beyond their programming skill obtained from the course entitled C for Engineers. However, before carrying out experiments, a well detailed tutorial of C programming is lectured and this process continues throughout the semester when it is needed. In addition, the lab course does not force them to learn the programming language strictly. Therefore, experiments, assignments, and projects are allowed to be done with team work. Also, grading policy does not only depend on the accuracy of software implementation. It actually relies on student effort and how seriously the lab course is taken.

The last thing that can be added to students' concern is that while taking this course they encounter a challenging face of the engineering world. Some of them think that they are not ready for this challenge.

V. CONCLUSION

The embedded system laboratory course, developed in the department of electrical engineering at the USF, intends to provide an engineering system approach throughout the learning experience. One of the goals is to create a culture among the students to properly meet the challenges encountered in embedded systems hardware and software design; but most importantly, the lab serves as a vehicle to prepare new graduates for the engineering workforce, placing them in high demand due to their competencies in embedded design. Evaluation results show how this new lab course extends students' engineering vision, and respond to enhancements of the mentioned challenges. Other institutes that wish to establish an embedded system based laboratory course can benefit from the content and the methodology ~~of~~ that the lab course offers. The proposed lab course inspires students and keeps them motivated in the embedded systems world. As a last point, since it is complimentary to the traditional theoretical courses, it can serve as a resource for students to create design projects.

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Energy Efficient Sensor Management Strategies in Mobile Sensing

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Abstract *— Mobile device based human-centric sensing and participatory sensing provide a vast context about the user state information. To capture and recognize any user state, then to classify it requires operating all existing sensors in a mobile device continuously. Nonetheless, constantly running sensors drain the mobile device's battery rapidly. Therefore, it is imperative to construct a framework to utilize sensors efficiently and try to recognize user states very accurately by consuming less power. In this paper, some strategies are proposed to correct the mentioned deficiency. It is aimed to detect and recognize user state transitions by first decreasing computational complexity during data processing stages, prompting time-varying efficient duty cycle schedules and setting adaptive sampling time periods to satisfy trade-off between accuracy vs. energy consumption.*

Keywords*:* Energy Efficiency, Mobile Sensing, Sensor Management Strategies, Ubiquitous Sensing.

I. INTRODUCTION

Nowadays, mobile phones are powerful devices since they are not only used for their fundamental purposes like calling or texting but also used for browsing the Internet, recording voices, taking instant snapshots, tracking any geo-location and so on. These mobile phones manage to perform these kinds of rich features using their on-board sensors like the accelerometer, Bluetooth, camera, GPS, microphone, Wi-Fi, and etc. Therefore, they are introduced to electronics consumers as smart phones. Due to technological advances and consumer demands, it is likely that consumers will anticipate and expect future smart phones to have more sensors and more sensor-based applications.

By utilizing sensors, some meaningful information about user locations, routines and surroundings can be extracted in real-time, allowing some applications to adapt to constantly changing environmental conditions and user preferences. As an example of the user activity sensors, an online application can be used for socializing platforms to update current user locations so that user followers can track the user.

Continuously capturing user context and extracting information make the mobile phone very busy, which causes it to draw a great deal of current from the device battery. This consequence will be very detrimental when powering more than one sensor. As a result, the device battery would die very quickly. It has been reported [1] that today's mobile devices are not durable enough to use all sensors at the same time, giving an example of the Nokia N95 mobile phone with a new fully-charged battery. It experimentally examined that the phone would be totally drained within six hours if the GPS was switched on permanently even when not being actively used; whereas the phone supported telephone conversation up to ten hours. In summary, to be able to run context extracting applications, energy saver algorithms must be considered and applied.

The best energy saving algorithm would consist of powering a minimum set of sensors to recognize any user state transition. Assigning different operation duty cycles to different sensors is proposed in this method so that at any time, there might be some sensors running, while others might be shut down. For example, if a user stays in-doors, there would be no reason to power-up the GPS sensor while accelerometer and Wi-Fi might be open. A novel approach would also be to change the duty in cycles, which means tuning the percentage of Logic '1' statuses of active wave forms, which power a sensor. Suppose that user is reading a book

and as time passes by, the activity of the user will become less, except for sitting. In this case, active time for powering the accelerometer to recognize body movement can be shortened.

Besides adjustable duty cycles, adaptively changing sampling periods is another novel approach to the problem. A mixture mechanism for utilizing the combined pair assignments of different duty cycles and sampling periods would be a cure for consuming less energy for user state recognitions. Looking at the previous example (the user who reads a book), if the user suddenly starts to sleep, there is a great probability of user's body movement reaching almost zero until waking. Also supposing there are some limitations such as the upper or the lower level percentage of duty cycling, then when time passes by, due to non-activity (the same user state all the time), the duty cycle will go down below the lower level. However, the mechanism should not let this happen, and can then change the current sampling period and enlarge it by keeping the current duty cycle fixed. On the other hand, an opposite example would be reaching above the upper level, and this time sampling period would be shortened. Unfortunately, this mechanism cannot be adapted to every sensor since those sensors must run under some dedicated transmission protocols. For example; Bluetooth, GPS and Wi-Fi are inside of that category of sensors while the accelerometer, microphone, and camera are not.

Reducing power consumption for the system operation perspective does not mean that recognition of user state transitions is not concise. There is a challenging tradeoff between power consumption and accurate user context extraction. While providing less power consumption, the system has to be sure that the current user state is accurate and any state transition is detectable. Most importantly, due to the duty cycling approach, some user state(s) might be missed. The system also has to be sure that these missing user state transitions are estimated.

This paper addresses novel approaches to solve the complexity of the trade-off, and represents them in detail. Proposed methods are summarized as follows: First, after each sensor reading, before recognition of user states, a sensor-specific buffered-feedback decision maker is employed. For some sensors like the accelerometer or GPS, a threshold value should exist, which can be seen as an inertia value, for finding out any change of current user state. Threshold is used to compare newly captured samples with previous samples stored inside of the corresponding sensor-specific buffer. For other sensors like the microphone or Bluetooth, a specialized digital signal processing block is needed to anticipate the information of no status changes in user states without performing more complex processing algorithms. Secondly, to recognize any user state, a minimum set of sensors is selected. Each sensor has its own different operation methods which are based on a set of time-varying duty cycles and a set of time-varying sampling periods (fast, normal or slow sampling periods). Therefore, according to each selected sensor, the energy cost estimation is done before beginning the sensor operation. Then, the selected sensor begins to operate. Operation duration and frequencies can alter in time.

II. SUMMARY OF PRIOR WORKS

There are a fair number of works which have been proposed for mobile sensing to recognize user states accurately enough by trying to consume less power; however most of those works provide only partial answers to the tradeoff between data accuracy and less power consumption, and there has not been much work done for constructing a total framework. At this point, it is worth mentioning that Wang *et al*. [1] proposes a sensor management system, which is called Energy Efficient Mobile Sensing System (EEMSS). The system improves device battery life by powering a minimum set of sensors and applying sensor duty cycles. However, sensors have fixed duty cycles whenever they are active, and they are not adjustable to different user behaviors. The same authors in [2] study how sensor duty cycles can be optimized in order to minimize the expected user state estimation errors while maintaining an energy consumption budget. The hierarchical sensor management system is also studied by introducing "SeeMon" system in [3] which achieves energy efficiency and less computational complexity by only performing a continuous detection of context recognition when changes occur during the context monitoring. Moreover, to find a solution for the tradeoff, the advantage of a dynamic sensor selection scheme for accuracy power tradeoff in user state recognition is demonstrated in [4]. Rachuri *et al*. [5] also uses

different sampling period schemes for querying sensor data in continuous sensing modes in mobile systems to evaluate energy-accuracy tradeoffs. This solution makes an attempt to solve the problem, but at this time for localization applications the results can be found as follows: At first, "SenseLess", described in [6], is a system for saving energy consumption by sensing localization applications for mobile phones. Then, Constandache *et al*. [7] studies energy efficiency in mobile device based localization, and the authors show that humans can be profiled based on their mobility patterns and thus location can be predicted. The proposed "EnLoc" system achieves good localization accuracy with a realistic energy budget.

III. PROPOSED STRATEGIES FOR ENERGY EFFICIENCY

Mobile phones today have a number of sensors which are capable of actualizing interesting applications. However, updating new features into these devices brings about some limitations on their battery life. Therefore, sensors which are constantly employed by any application can cause high power consumption per time unit compared to what they do while a telephone conversation is being made. In [6], the approximate effect of present-day mobile phone sensors on device battery life is investigated by experimentally finding out their average power consumptions when they are individually turned on. According to the results, the least power consuming sensor is the accelerometer. The Bluetooth, microphone, GPS, Wi-Fi and video camera follow accelerometer respectively. Therefore, the best battery-care approach would be that user state recognition based applications should start their operations by using the accelerometer as a default sensor.

In this paper, there are two model approaches proposed for improving the tradeoff between power consumption and accuracy of user state recognitions. The first approach is called a context monitoring mechanism, which basically considers the achievement of energy efficiency in a computational manner; and the second one is called an adaptively sampling and duty cycling method, which aims to obtain energy efficiency in a physical manner while sensors are being operated.

A. Context Monitoring Mechanism

A major challenge in extracting user contextual information is based on monitoring the context continuously. Constantly context monitoring in a sensor-rich mobile phone imposes heavy workloads which cause some limitations in computing and battery power. Therefore, there should be a mechanism to organize required processes for analyzing the context in such way that redundant repetitions of the same contextual information can be avoided.

Once a transition occurs in a new user state, there is no necessity of recognizing and notifying the same context (existing of same conditions) redundantly again and again as long as the user state remains unchanged. A mechanism can be considered to elaborate computational complexity during the processing of a sensor data; as a result, a decision on the continuity of user states can be made at an early age of the total processing pipeline by achieving significant computational overhead save.

As illustrated in Fig.1, detection of user contextual information is recognized by employing an intelligent computational method. It is aimed at performing an inexpensive strategy without completely exploiting a raw sensor data to make the decision on the continuity of current user state.

The conventional user state recognition method tries to process and analyze raw sensor data, exploit context information, and compare it with a classification algorithm based on decision tree logic. In this method, almost all raw sensor data is carried through a processing pipeline, and ends with a user state decision. In the proposed approach, an intelligently pipelined context monitoring mechanism is introduced to reduce the high cost for required operation sequences. The main objective of the mechanism is to notify user states of a running application only when a user state transition occurs.

In Fig.1, the sensor produces a discrete raw data periodically. The data enters into a processing pipeline; output of the pipeline is to inform possible change of user states or not since the data is found to be identical to previous ones which were buffered.

The pipeline starts with a preprocessing structure. This structure basically filters out the required information from the raw sensor data. The information varies from one sensor to another. For example; the accelerometer and microphone give away only one part of the required information whereas Wi-Fi and GPS return a package that includes different kinds of information. Therefore, there might exist more than one piece of monitored information sent by the sensors. Different amounts of contextual information forces it to have the same number of information buffers. Each buffer has the same kind of contextual data which belongs to previous samplings. Buffers are designed to gain flexibility and speed on decision making, and also, most importantly, to help in decreasing the number of redundant computational operations which can yield to stopping the pipeline before feature extraction algorithms are applied. For example; let us imagine that the accelerometer converts an analog signal and returns related discrete digital data a hundred times in a second. Since any user state cannot be changed drastically that sensor misses transitions, there is no point of processing all algorithms at each sensor reading, and then send detected user state information to running application all the time. At that point, a tradeoff might come up for buffer size that resolves the accuracy of the decision on deciding current user state.

Buffers consist of comparison variables which are obtained from statistical analysis on the previously stored contextual information. Comparison variables can be standard deviation, variance or any other result of applied statistical tools. At the middle stage of the processing pipeline, decision maker classifications are applied among current and previous contextual information to interrogate the existence of future processes such as feature extraction. The feature extraction block is the place where new and different contextual information is exploited to bring about a possible user state transition. For instance; if an environment is detected as silence before, and if newly obtained data indicates there is a changing situation in environmental context, the feature extraction block analyzes the data and sends out the resulting outcome to the user state detector block to decide on which user state will be selected. Would it be ‘loud’, ‘music’ or ‘speech’?

The user state detector block recognizes user state transitions, and informs the applications. Another important property belonging to this block is to assign a required sensor set for the recognition of current user states and possible user state transitions.

The duty cycle and adaptive sampling adjuster block keep tracking the length of time intervals in which sensor readings do not yield that cause it to miss any user state transition. Therefore, depending on how long time is spent on a user state, duty cycles and adaptive sampling periods can be adjusted to secure energy efficiency.

Lastly, the application is notified when a user state transition occurs. It also queries the mechanism any time a user defined event is wanted to be queried to check whether it might be happening or not.

B. Adaptively Sampling and Duty Cycling

Sensors on a mobile phone can be categorized into two classes depending on their operation styles. The first class includes the accelerometer and microphone. These sensors are turned on once to operate continuously; they need an external command to finish their operations and to become turned off. They both require an optimal minimum sampling period to capture meaningful contextual user information. The corresponding sampling period to each sensor can be adaptively changed in case some power considerations are taken. The second class of sensors includes GPS, Wi-Fi and Bluetooth. When these sensors are turned on, they automatically turn into the idle position after the required sensing operation is done. Also, there are some dedicated transmission protocols that these sensors must follow to accomplish their operations. Therefore, they might be unable to run them under different sampling periods. Although Bluetooth is employed in the second class while scanning nearby users, it may be also considered a member of the first class as well while its spectrum is being sensed and analyzed with different sampling periods.

1) Sensor Operation Structure

The energy cost of any sensor does not only depend on instant energy consumption per operation, but also on the duration of the operation itself. In Fig.2, sensor operation structures for both classes are illustrated. This structure starts with an

initialization block, and that block deals with waking the sensor up and then waiting for an acknowledged response which informs that the sensor is ready. For example; the study in [1] states that for GPS functionality, it requires at least 10 seconds to successfully synchronize with satellites. For other sensors, a shorter time period would be sufficient to power them up and to set their initial system requirements before sampling operations begin. The second block is called processing. This block is dedicated to providing efficiency in energy consumption. In this block, the sensor starts to capture user contextual information and continue on this operation repeatedly. The third block ends the active duty of the sensor, and terminates it. After all these three blocks, the sensor shuts down until a new duty is assigned.

The processing block is the place where the duty cycle length and sampling period are adjusted dynamically for a sensor. Energy consumption is reduced by carefully assigning a pair of the duty cycle and sampling period. However, these assignments are going to cause a tradeoff between reduced energy consumption and accurate sensing. If successive sampling intervals are too long, there

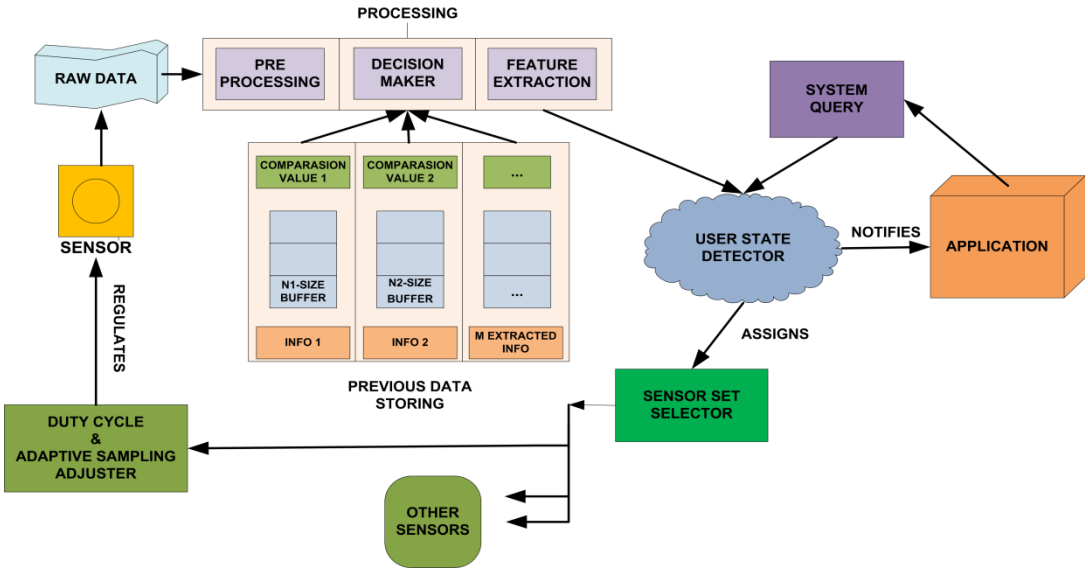

Figure 1. Context Monitoring Mechanism

would not be sufficient samplings to present real conditions, and eventually it would cause it to sense user contextual information incorrectly from the sensed data. On the other hand, in the case that the intervals are too short, energy saving would not be satisfied. The same approach can also be applied to sensor sleeping time intervals as well. A longer sleeping time interval would reduce energy consumption; nonetheless, detection latency will be increased so that false detections could occur.

2) Preliminaries and Construction of the Proposed Approach

Assuming that an application needs to employ a sensor, and β_{total}, t_{total} and t_c are given for the application as the total energy budget for accomplishing all sensing operations, the total active time for the sensor and the corresponding time to drive a sensor per a cycle respectively. ϑ_{sample} and ϑ_{idle} are also given as constant default sensor properties for energy consumptions to sense a contextual data per time unit and to run with no operation while being idle per time unit respectively.

A novel approach is applied to the sensor, which enables it to change the duty cycle of active sensor prompting signal and sampling periods adaptively during sampling operations being executed. Therefore, a set of duty cycles and a set of sampling frequencies need to be introduced to the system.

$$DC(i) = [\ 0.2, 0.4, 0.5, 0.6, 0.8\ ] \qquad (1)$$

DC(i) is a required set for duty cycles. It is limited to 20% for the lowest level because below this level would bring high risk for recognizing user states accurately enough. On the other hand, at above 80% would help to recognize user states much more accurately has and avoid having energy wasted unnecessarily.

$$Fs(j) = [\, fs_{slow2}, fs_{slow1}, fs_{normal}, fs_{fast1}, fs_{fast2} \,] \quad (2)$$

Different sampling frequencies are introduced into the system inside of a set called *Fs*(*j*).

With the combined existence of *DC*(*i*), *Fs*(*j*), and t_c, the number of occurrences of sampling operations inside of an active cycle can be calculated as follows:

$$N(\, i, j \,) = (\, DC^{\,T} \, x \, Fs \,)\, t_c \quad (3)$$

N(i,j) is a [*length of DC(i) x length of Fs(j)*] matrix which gives various numbers of sample operation when a specific *i* and a specific *j* are selected together by the system. As illustrated in Fig.2, t_{run} can be extracted as:

$$t_{run} = t_{total} - (t_{init} + t_{term}) \quad (4)$$

Due to the fact that duration of t_{init} and t_{term} are approximately constant all the time for a sensor, the value of t_{run} yields to have the number of running active cycles during the processing block is active.

$$N_{run} = t_{run} / t_c \quad (5)$$

With the knowledge of how many times active cycle runs during processing and how many times sampling occurs inside of each active cycle, total energy consumption, θ_{run}, can be estimated.

$$\Theta_{run} \approx \sum_{n=1}^{N_{run}} \Big[\Big(\sum_{k=1}^{N(i=selected, j=selected)} \delta(k)\vartheta_{sample} \Big) + (1 - DC(i = selected))t_c\vartheta_{idle} \Big] \quad (6)$$

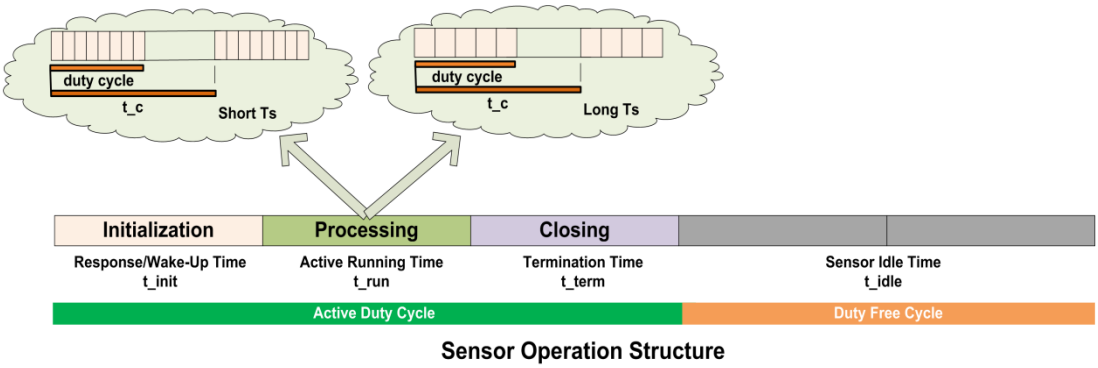

Figure 2. Adaptively Sampling and Duty Cycling

Note that idle times between two consecutive samplings are ignored; and for the calculation of energy consumption during idle times, continuous time is used; whereas, for the calculation of energy consumption at sampling times, discrete time is used.

Since the proposed approach adjusts a combination pair of the duty cycle and sampling frequency adaptively as each active cycle runs, the number of samples inside an active cycle is also changed adaptively. Thus, energy consumption at active task differs at each cycle. Plus, energy consumption of idle task also differs because of various duty cycle selections. As a result, total energy consumption will depend on aggregation of total wasted energies at every cycle.

The proposed method aims to consume less energy than given β_{total} as an ultimate goal. Assuming that θ_{init} and θ_{term} are energy

consumptions while sensor is initializing and terminating, the required inequality becomes:

$$\theta_{init} + \theta_{term} \approx (t_{run} + t_{term}) \vartheta_{idle} \quad (7)$$

$$\beta_{total} \geq \theta_{init} + \theta_{run} + \theta_{term} \quad (8)$$

The efficiency, ζ, gained after less energy consumption from anticipated energy budget, β_{total}, is calculated as:

$$\zeta = \frac{\beta_{total} - (\Theta_{init} + \Theta_{run} + \Theta_{term})}{\beta_{total}} 100\% \quad (9)$$

IV. FUTURE WORK

Integration of the proposed method related to adaptively sampling and duty cycling, implementation of possible algorithms and simulation of them are considered as a future work for this study.

V. CONCLUSION

Novel approaches are introduced in this paper, which attempt to control mobile phone sensors in such a way that correct user state recognitions are still obtained while reducing energy consumption. The paper includes important information on how the system framework should be constructed and modeled.

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