Experimental Platform in Digital Control of DC-DC Converters

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Abstract — This article describes the implementation of a platform for experimentation in Digital Control of DC/DC Converters. This platform will allow us to discuss different techniques for power converters control, assess the state of the art and propose new techniques for specific applications in chip development or electronic systems. The platform consists of a DC/DC Buck type converter, two variable resistors, four A/D converters and a PID controller developed in an FPGA. The modular design allows us to add different converters, fillers and methods of control.

Keywords: A/D Converter, Analog-digital conversion, Buck Converter, DC/DC Converter, DC-DC power converters, Digital control, Dynamic load, FPGA, Switching converters.

I. INTRODUCTION

This article describes the construction of an experimental hardware platform, consisting of power converter modules and a digital controller module.

The power modules (DC-DC regulators, AC-DC rectifiers and DC-AC inverters) cover a range of low, medium and high power applications and have already produced some successful commercial products [1,2,3]

The purpose of this project is to consolidate a working group to develop techniques for modeling and to allow the control of switched circuits, especially in power electronics applications for effective and efficient conversion of electrical energy.

This work is part of a CSIC[1] project of research and development to consolidate the control group of power electronic converters.

The power modules (DC-DC Regulators) cover a wide range of applications of low and medium power, particularly for voltage regulation in portable electronic systems and computer equipment. The controller module is based on an FPGA with a PC programming interface.

II. FUNCIONAL SPECIFICATION

The system consists of a digital control module implemented with an FPGA[2] on the card IIE-Cyclone-II[3] [4, 5] and three types of peripherals: Resistive Dynamic Load, A/D Converters and two DC/DC converters, one Buck single phase converter and one Buck multiphase converter.

The control module and peripherals are the experimental platform of digital DC/DC control converters.

The FPGA will be responsible for performing the digital control of DC/DC converters and for analyzing the data from the output voltage and current of DC/DC converters that come through the A/D converter, while controlling the output voltage. Another task of the FPGA is to determine the dynamic load value commanded from the PC.

The single phase converter converts 5V to 3.3V and works up to 10A of current. The multiphase converter, converts from 12V to 1,5V up to a maximum current of 50A.

The A/D converter reads the tension or the current of the converter and sends the correct digital word to the FPGA.

The Dynamic resistive load receives a binary word from the FPGA and generates a combination of resistances. It is responsible for control of the dynamic demand for power to the DC/DC converters.

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[1] In Spanish: Comisión Sectorial de Investigación Científica, UdelaR

[2] Field Programmable Gate Array
[3] It is the final product of another IIE project based in a Cyclone-II card of ALTERA [5,10]
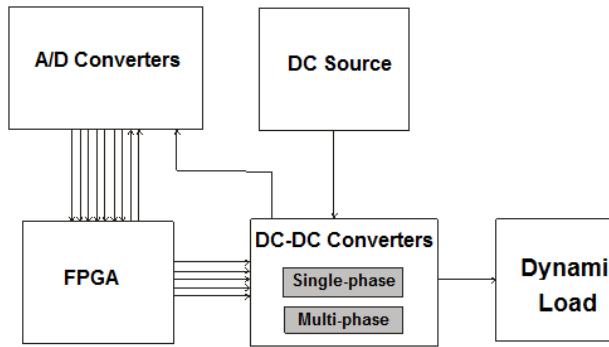
Figure 1. Dynamic load block diagram

III. DESIGN

A. Resistive Dynamic Load

In order to test the DC/DC converters, resistor values between 0.016Ω and 50Ω are needed. However, there are plans to work in two more DC/DC convertors, so another range of loads between 50Ω and 40KΩ was considered.
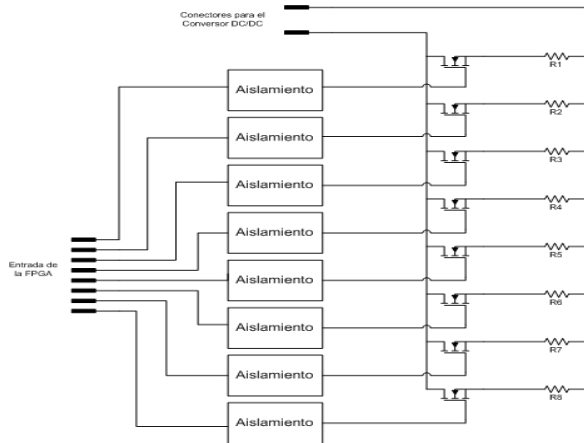

Figure 2. Dynamic resistive load scheme

There are only 8 bits of the FPGA available for changing the load, so some values were chosen to work in the adequate range.

TABLE I
FIRST RANGE OF LOAD VALUES

Word	Value (Ω)
00000001	0.02
00000010	0.33
00000100	1.50
00001000	4.00
00010000	10.00
00100000	20.00
01000000	40.20
10000000	50.00

TABLE 2
SECOND RANGE OF LOAD VALUES

Word	Value (Ω)
00000001	50
00000010	100
00000100	500
00001000	1000
00010000	8200
00100000	13000
01000000	30000
10000000	40200

In Figure 3, a schematic of how to perform the control of the MOSFETs transistors with the FPGA, which delivers a voltage of 3.3V, is shown. This voltage passes through an optocoupler to isolate the FPGA from the rest of the circuit, then a driver to adapt the signal to the MOSFET.
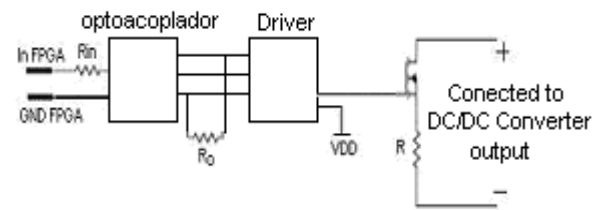

Figure 3. Load branch scheme

R_{in} resistance works both by limiting the current that is required for the FPGA and by supplying enough current to power the diode.

As a means for testing the loads, the pins for the FPGA were connected, binary words from the PC were entered, and the value of output resistance was checked. The results are shown in Table 3 and 4.

TABLE 3
FIRST RANGE OF LOAD EXPERIMENTAL VALUES

Word	Theoretical Value (Ω)	Measure Value (Ω)
10000000	0.030	0.4
01000000	0.33333333	0.53
00100000	1.5	1.7
00010000	5	5.18
00001000	10	10.29
00000100	20	20.32
00000010	40	40.45
00000001	49.9	49.96

TABLE 4
SECOND RANGE OF LOAD EXPERIMENTAL VALUES

Word	Theoretical Value (Ω)	Measure Value (Ω)
10000000	49.9	49.8
01000000	100	99.8
00100000	560	559
00010000	1000	998
00001000	8200	8140
00000100	13000	12970
00000010	30000	29900
00000001	40200	40000

B. A/D converter

Figure 4 shows the stage of the signal and the A/D converter conditioning in a block diagram. Adaptation of the signal of interest from the DC/DC converter to the range of values that the A/D converter can handle will occur during this stage.

Figure 4. A/D converter block diagram

As a first step a boost or reduction of the input voltage was implemented, being necessary to encompass the whole range of the converter. In a second step the signal is filtered by a low pass filter (LPF Low Pass Filter) with a cutoff frequency (fc) less than half the sampling frequency (fs) of the converter, to eliminate the aliasing effect. Figure 5 shows a block diagram of the conditioning step.
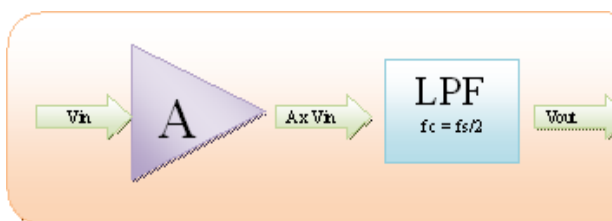

Figure 5. Conditioning step diagram

Conditioning requires different types of boost or reduction, which were implemented by means of mechanical jumpers.

TABLE 5
A/D CONVERTER AMPLIFICATION GAINS

Vi	Gain	Vo
1	1	1
1.5	2/3	1
10	1/10	1
20	1/20	1

Signal filtering is performed using an active filter of first order with cutoff frequency at 1MHz. It is shown in the diagram in Figure 6.
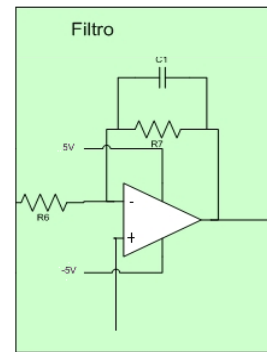

Figure 6. Anti-aliasing filter

In order to get a good resolution, a 10 bit Texas Instruments ADS822E converter was chosen, with 40MSPS sampling rate and a latency of less than 0.5 us.
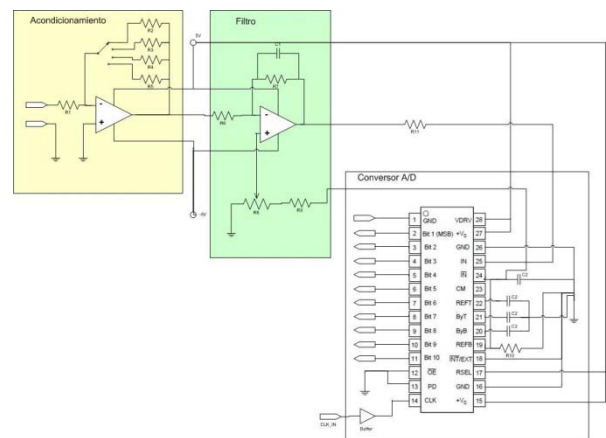

Figure 7. Common mode A/D converter diagram

Figure 7 shows a converter diagram with

common mode input. This converter allows us to measure the DC/DC converter output with greater precision.

Figure 8 shows a diagram of a differential input converter, its configuration allows measuring voltage or current values of any component since it can take negative values.
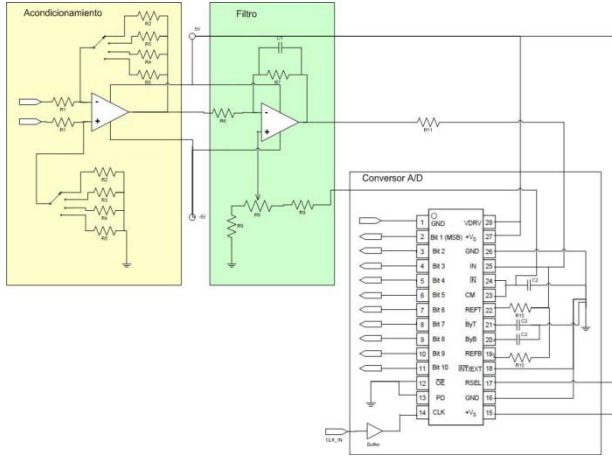

Figure 8. Differential input A/D converter diagram

Test results are shown in Figures 9 and 10. They are average values obtained by the FPGA.
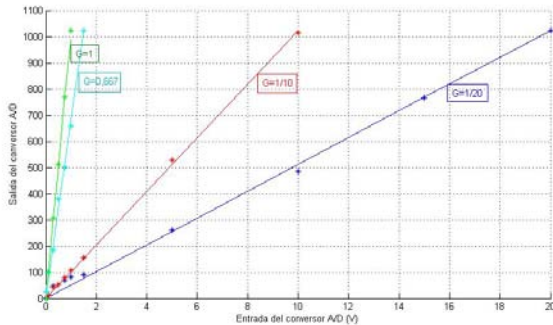

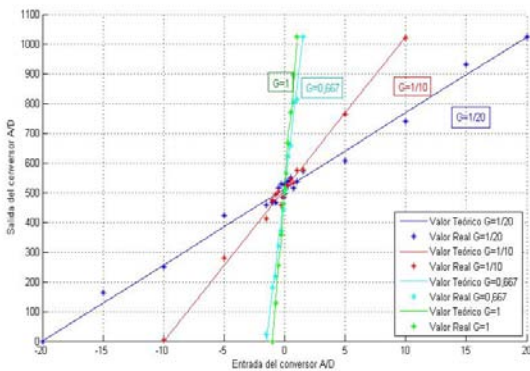Figure 9. Test input common-mode converter.

Figure 10. Test input differential-mode converter.

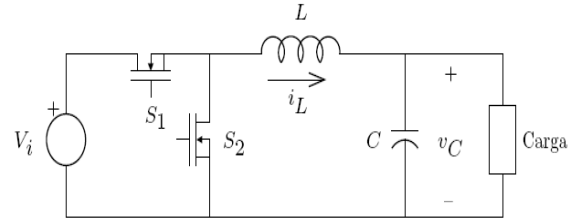## C. DC-DC Converters

Converter Buck single-phase

Figure 11. Single-phase DC/DC Converter Scheme [7]

In Figure 11 a basic diagram of the single-phase Buck converter is shown. To calculate the components values, three principles of the system in regime were taken into account:

1) *Volt • Second Balance: the average value of the applied voltage on an inductor must be zero.*

2) *Load balancing: the average value of the current through a capacitor must be zero.*

3) *Small ripple assumption; we can approximate the voltages on the capacitors at their DC values, and in some cases, approximate the currents by inducing their DC values (though for instance, this is not true in DCM). [7]*
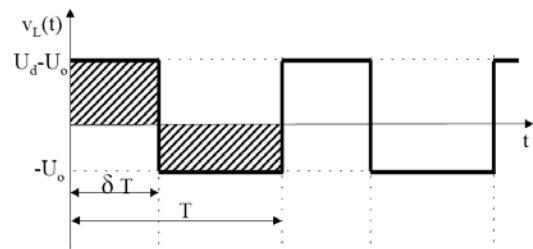

Figure 12. Voltage applied to the inductance. [6]

In Figure 12 the voltage applied to the inductance of the filter is shown. Applying the first hypothesis the average voltage on the inductor is taken as zero:

$$\langle v_L \rangle = \frac{1}{T} \int_0^T v_L(t)dt$$

$$= \frac{1}{T}\left[(U_d - U_o)\delta T - U_O(1-\delta)T \right]$$

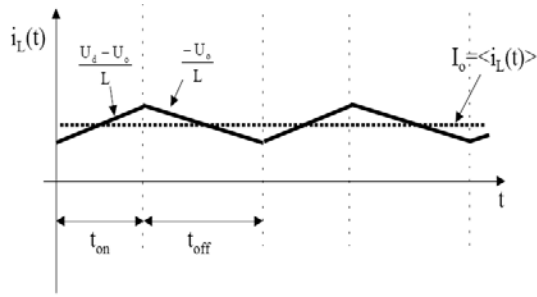$$U_d \delta - U_O = 0 \Rightarrow \frac{U_o}{U_d} = \delta \ (1)$$

Figure 13. Current through the inductor

Figure 13 shows the current in the inductance. Equation (2) can be derived.

$$\Delta I = \frac{U_d - U_o}{L} \delta T \text{, and being } \frac{U_o}{U_d} = \delta$$

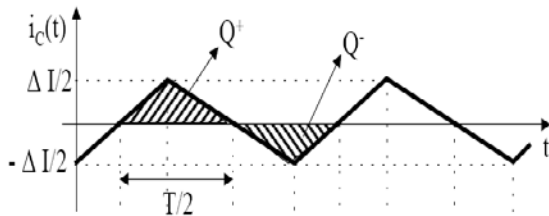$$\text{then } \Delta I = \frac{U_d T}{L} \delta (1 - \delta) \quad (2)$$

Figure 14. Current through capacitor [6]

In Figure 14, ΔI represents the ripple current from the capacitor (and therefore inductance) and Q+ and Q-, the maximum and minimum loads, respectively, which the capacitor will have.

To calculate the output ripple voltage of the converter, the maximum accumulated charge on the capacitor Q+ is to be considered. Then in Figure 14 we have:

$$v_C(t) - v_C(t_0) = \frac{1}{C} \int_{t_0}^{t} i_c(t) dt$$

$$\Delta v_C = \frac{1}{C} \frac{1}{2} \frac{T}{2} \frac{\Delta I}{2}$$

Substituting in equation (2):

$$\Delta v_C = \frac{T^2}{8C} \frac{U_o}{L} (1 - \delta) \quad (3)$$

Defining: $\omega_C = \frac{1}{\sqrt{LC}} = 2\pi f_C$ and $f = \frac{1}{T}$ the

following expression is obtained for the relative output voltage ripple:

$$\frac{\Delta v_C}{U_o} = \frac{\pi^2}{2} (1 - \delta) \left(\frac{f_C}{f} \right)^2 \quad (4)$$

Considering the real capacitor model as an ideal capacitor in series with a resistance and if it is significant, the output voltage ripple can be approximated by $\Delta v_C = V_{ESR} = R I_o$

For the converter design, the output voltage ripple was considered to be less than 5%, the ripple of the current must be less than 30% of the maximum current Io, and work will be performed with a value of T = 1.28ms.
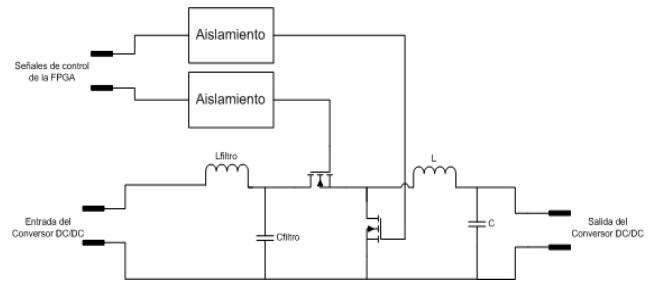

Figure 15. Single phase converter diagram

The single-phase converter converts 5V to 3.3 V and using equation (1) the following was obtained:

$$\Delta v_C \leq 0,1 \ 6V5 \text{ y } \delta = \frac{U_o}{U_d} = \frac{3,3V}{5V} = 0,66$$

Substituting these values in the equation (4) and working out LC, it can be found that:

$$L \ C \geq 1,4 \times 1 \ 0^{-1 \ 2} \quad (5)$$

The converter was designed for a range of 0.1 A to 10 A, then the ripple current status is $\Delta I \leq 3A$. If this value is substituted in equation (2) the second inequality is found:

$$L \geq 0,4 \ 8 \ \mu H \quad (6)$$

From (6) y and (7) L = 0.5 μH y C=3 μH were chosen.

A filter consisting of an inductor and a parallel capacitor was placed in the input of the converter, this filter serving to isolate the equipment connected to the input from the noise

introduced by the switches.

Buck multiphase converter

The multiphase converter designed converts 12 V to 1.5 V, being similar to the single-phase one but with four inductors instead of one, switches being activated in out of phase by a quarter period, discarding the first order current harmonics and getting a smaller ripple.

As in the single phase converter, it can be calculated that:

$$\delta = \frac{U_o}{U_d} = \frac{1,5V}{12V} = 0,125$$

The current ripple for each branch of the converter must be less than 30% of the maximum current for each branch and a period of 1.28 microseconds was used.

As the converter was designed for a maximum load of 50 A and a 4-phase converter was desired, the condition of the ripple current in each branch is:

$$\Delta I = \frac{U_o T}{L}\left(1 - \delta\right) \le \frac{50A}{4} \times \frac{30}{100} = 3,75\ A$$

The condition to be met by the inductance of each branch of the converter is:

$$L \ge 0,4\ 4\ \mu H$$

To determine the capacitor value it is necessary to take into account that the output voltage ripple should be less than 5%, as in the case of single-phase converters.

$$v_C(t) - v_C(t_0) = \frac{1}{C}\int_{t_0}^{t} i_C(t)\,dt$$

$$\Delta v_C = \frac{1}{C}\frac{1}{2}\frac{T}{2}\frac{\Delta I_T}{2}$$

Being iC(t) and ΔI_T the current and the total current ripple through the condenser respectively. Therefore, in order to determine the value of C the only additional data needed is ΔI_T.

The current iC (t) is the sum of the currents through the four branches of the converter which are like those in Figure 14 but with offsets of 90° between them. While finding the sum, a periodic triangular wave is obtained. Figure 16 shows how the slopes of each leg of

the triangle wave - that results when the original function f (t) have slope "a" in (0. δT) and "b" in (δT.T) for the four possible cases: 0<δ<0.25; 0.25<δ<0.5; 0.5<δ<0.75 and 0.75<δ<1 - are.
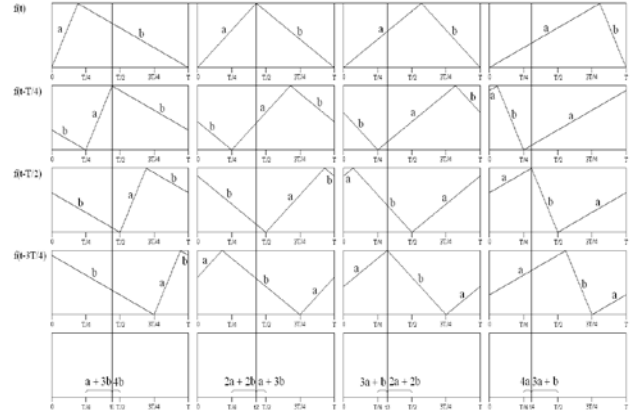

Figure 16. Currents through the branches of the multiphase converter
.

The resulting wave frequency is four times bigger, so the period is 0.32 microseconds.

As in the case of the single phase converter, the duty cycle is 0.125.The case of the first column from the left of the figure above is studied, to analyze the total current.

Having chosen an inductance value of 0.51μHy, the ripple voltage in each branch is 3.29A. Therefore:

$$a = \frac{\Delta I}{\delta T} = \frac{3,2\ A}{0,1\ \times 1,2\ \mu s}\frac{9}{58} = 2\ ,5\ A\ /\ \mu s \quad \text{and}$$

$$b = -\frac{\Delta I}{(1 - \delta)T} = \frac{3,2\ A}{0,8\ \times 1,2\ \mu s}\frac{9}{58} = -2,9\ A\ /\ \mu s$$

By means of these values the total current ripple is calculated as:

$$\Delta I_T = \left(a + 3b\right)\left(t_1 - \frac{T}{4}\right) = \left(a + 3b\right)\delta T$$

$$= 1\ ,7\ A\ /\ \mu s \times 0,1\ \times 1,2\ \mu s\ 58 = 1,8\ A$$

We can obtain C from the ripple voltage equation:

$$\Delta v_C = \frac{1}{C}\frac{1}{2}\frac{T}{2}\frac{\Delta I_T}{2}$$

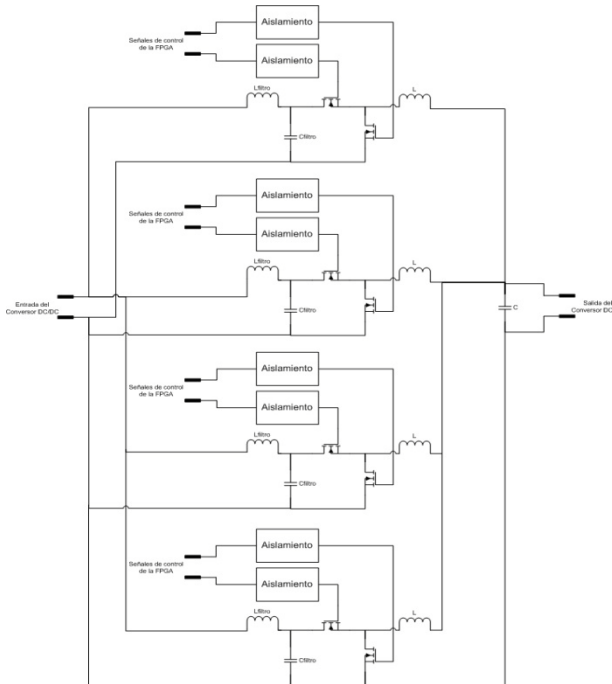Recalling the assumption that the output voltage ripple should be less than 5% we obtain that $C \geq 1,004 \mu F$

Figure 17. Multiphase converter scheme

D. *PWM signal generation for command DC-DC converters*

Implementation was performed in VHDL modules that were recorded in the IIE-Cyclone II card allowing the following:

1. Management of Dynamic Loads switch
2. PWM signal generation for the management of the DC/DC converter switches in open loop
3. Feedback output voltage DC/DC converters for closed loop test
4. Generation of clock signal for the A/D converter and the PID controller

In order to create the modules, a modulator implemented as a final project for the subject named Logical Design 2 was used as a reference [9].

The open loop system of the DC/DC converter takes the duty cycle of PWM signals that command the switches (represented by 10 bits) as inputs, and the voltage delivered by the converter as outputs (see Figure 18).
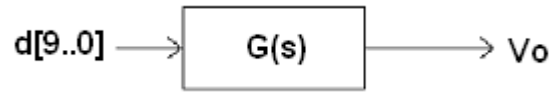

Figure 18. Open loop system

The system shall generate periodic waveforms with the duty cycle d[9..0] and shifted 90º, 180º and 270º between the different branches of the 4-phase converter as shown in Figure 19.
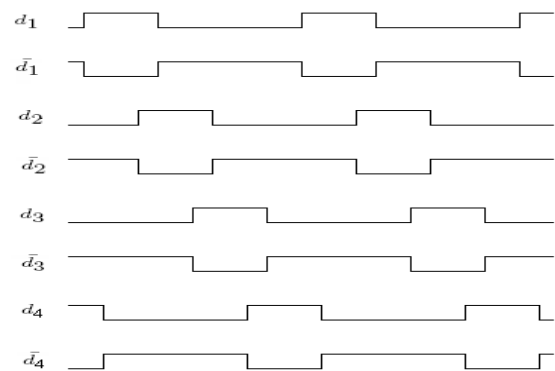

Figure 19. PWM pulses for keys management of a DC-DC multiphase converter.

The following section describes the implementation of a module from a previous work [9] that consists of a pulse width modulator with 10 bits to represent the duty cycle, as shown in Figure 20.
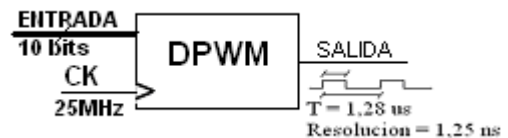

Figure 20. 10 bits Pulse width modulator

This modulator is based on the use of the 8 most significant bits of duty cycle in order to obtain a periodic wave but with 5 ns resolution. We used a counter with the output connected to a comparator, thus producing periodic wave "thickness adjustment".
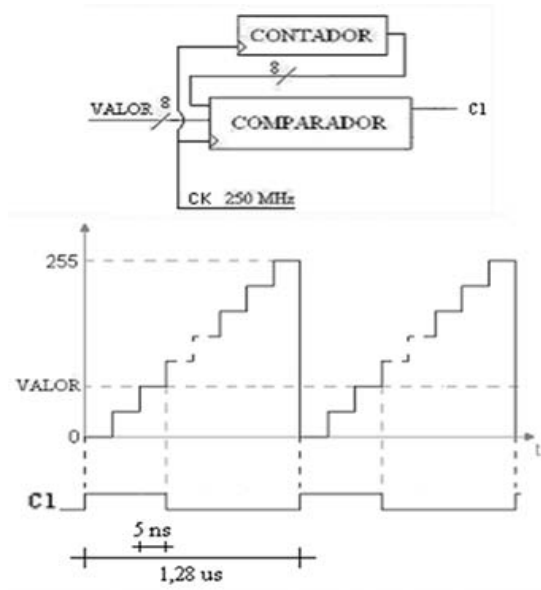
Figure 21. Thickness adjustment

For a resolution of 1.25 ns ("fine adjustment") the 2 less significant bits of duty cycle and a serializer were used.
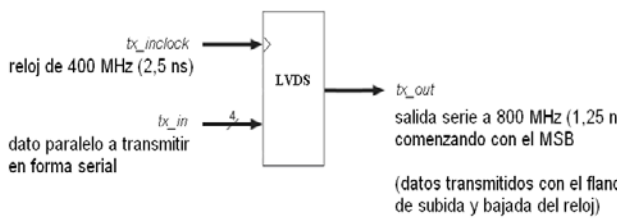

Figure 22. Serializer for fine adjustment

From the thickness adjustment wave and the 2 least significant bits, we can determine which bit and when to put it into the serializer in order to get a resolution of 1.25 ns.
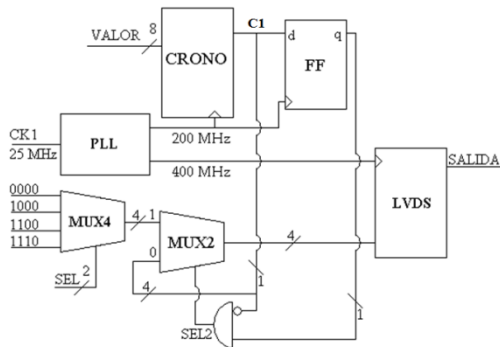

Figure 23. Modulator diagram ([9]).

DPWM

This block is based on the modulator described above and can also generate periodic "Inverse" waves and 90º, 180º and shifted 270º to handle all the switches of a 4 phase DC/DC converter.

The "inverse" waves are the theoretical duty cycle 1-d, where d is the duty cycle that determines the transformation ratio. In this case an additional parameter of 8 bits, SEPARATION, was introduced, which adjusts the inverted wave as shown in Figure 24.
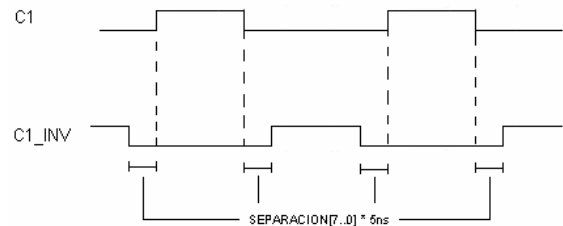

Figure 24. SEPARATION Parameter [7.0]

In Figure 24, C1 represents the periodic wave of thickness adjustment. With this parameter, the length of time that both switches are open simultaneously can be controlled. COMPARATOR INVERSOR block was implemented taking into account the parameter SEPARATION (8). Thus C1_INV gets a resolution of 5 ns.
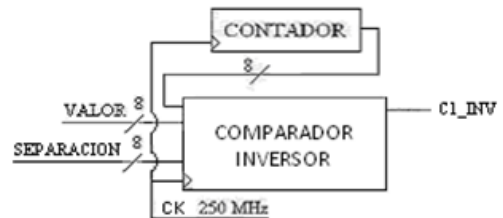

Figure 25. Blocks for generating of "inverse" waves

In order to obtain the shifted periodic waves, the block in Figure 26 was implemented.
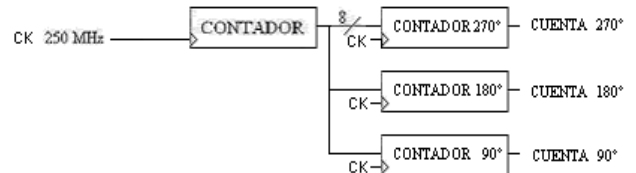

Figure 26. Blocks for generating shifted waves.

Shifted waves 90°, 180° and 270° with respect to a reference were obtained. With each of the counters, wave thickness adjustments were generated. Then higher resolution waves were generated as described above, obtaining

shifted waves with a resolution of 1.25 ns.

E. Control in FPGA implementation

The block for the feedback output voltage DC/DC converter is shown in Figure 27.
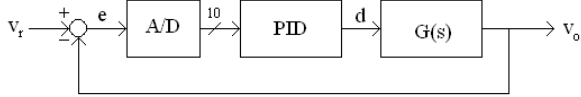

Figure 27. Output voltage feedback

Auxiliary signals were generated and a block for a PID control of the plant was done.

Recycled DPWM

This block is basically the DC/DC system described above with the addition of the following outputs, and a PID block (Figure 27):

CLK_ADC: clock signal period of 640 ns (a half of the PWM period). It is used in the A/D converter and the PID.

CE_PID: Signal for enabling PID block result readings. It is always high, so it only includes the rising edge of CLK_ADC that is half the PWM cycle.

CK_DPWM: clock signal with a period that equals the PWM signal (1.28 us) period but with the rising edge 160 ns before the end of the previous. It is used to load the reading of the DPWM block in the PID controller at the end of the PWM cycle, so as to avoid further changes at the logic level in the PWM signals in the same period.
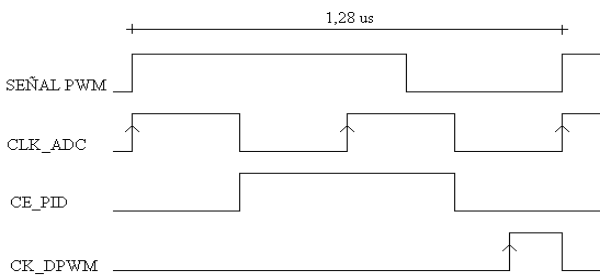

Figure 28. *Auxiliary signals for closed loop control.*

PID

The PID corresponds to the proportional-integral-derivative control of the output voltage of the converters in discrete time. Its entries CLK_ADC, KP, KI, KD and ERROR[9..0] correspond to the output of A/D converter. The output D[9..0] is of the form: $D[n] = KP*ERROR[n] + KI*(S[n-1] + ERROR[n]) + KD*(ERROR[n]-ERROR[n-1])$, where $S[n-1] + ERROR[n] = S[n]$ is the cumulative sum of the integral term and all the variables that are represented in two's complement.

In order to obtain $S[n-1]$ and ERROR $[n-1]$ (sampled values earlier than n) type D flip-flops with clock CLK_ADC were used (see following figures).
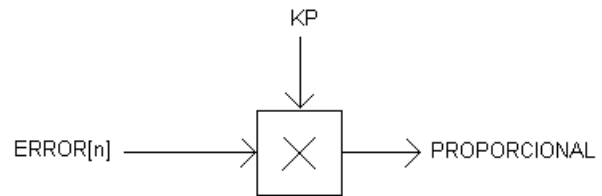

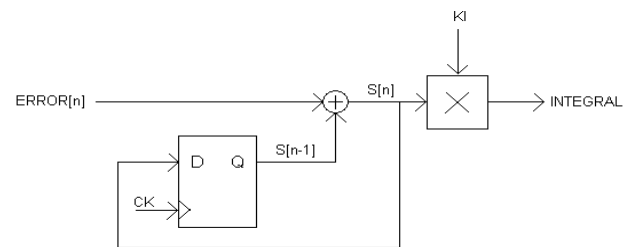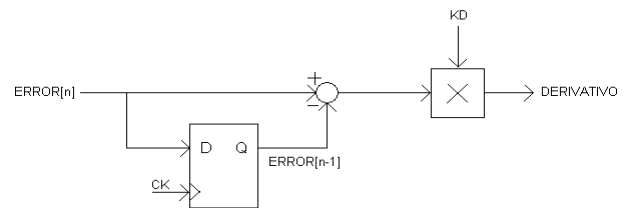Figure 29. Proportional block diagram

Figure 30. Integral block diagram

Figure 31. Derivative block diagram

To perform the multiplication and sum of the vectors of the relationship that defines D[n], configurable blocks existing in the Cyclone II chip are used.

The block that calculates the integral term is designed so that S[n] saturates at -2048 and in 2047.

For simplicity purposes, the detailed

calculation of the controller constants is not shown, the constants obtained being:

KP = 0.12628 KI = 0.06186 KD = 0.02596

As work is done on the binary system, it is approximated by:

KP = 0.001000 KI = 0.000011111 KD = 0.0000011010.

It was decided to work with constants of 6-bit with their format:

<1 bit of sign><2 bits>,<3 bits> for performing the operations in the controller with a fixed number of bits regardless of the values.

Therefore, for the above values, a shift of the dot of 1, 6 and 6 places to the right for KP, KI and KD was applied respectively, then obtaining the following constants in the format explained above:

KP = 000.010 KI = 011.111 KD = 001.101.

With this format for the constants and taking into account that ERROR is 10 bits and S (sum of the integral term) is 12 bits, the proportional term gets the form: <13 bits>,<3bits>; the integral <15 bits>,<3bits> and the derivative <13 bits>,<3bits>.

Now, we must undo the shift of the dot applied to the constants. So the format of the proportional term is: <12 bits>,<4 bits>; the integral <9 bits>,<9 bits> and the derivative <7 bits>,<9 bits>.

To make the sum of the three terms, they must be in the same format: <12 bits>,<9 bits>.

Therefore it may be necessary to extend the decimal bits by adding zeros to complete 9-bit and make a sign extension to complete the entire 12 bits (repeating the sign bit as many times as necessary to be a two's complement).

The result of the sum is obtained in the form: <14 bits>, <9 bits> (there are 2 additional bits for the case of carry). D (duty cycle) is obtained from the fractional part of the sum, taking into consideration:

1. If the integer part is > = 1, then D = 1111111111 (1023)
2. If the integer is negative, then D = 0000000000 (0)

3. Otherwise, D is the fractional part of the sum by adding a zero to make 10-bit LSB

IV. PLATFORM TESTS

The following tests were performed: response to the variation of duty cycle, response to load variation, and transient test.

In this article, only the test of the single-phase DC/DC converter is presented, having postponed the multi-phase test for a second stage.

The test of the response to the duty cycle variation consists in taking samples of the voltage of the converter output, with constant input voltage and load. We did the test with an input voltage of 5V and a load of 1kΩ.

The duty cycle is changed from 0.1 to 0.9 taking 11 samples of the output voltage. In Figure 32 the output voltage obtained is plotted as a function of duty cycle, and it can be noticed that the graph is monotonic and pretty close to the ideal line.
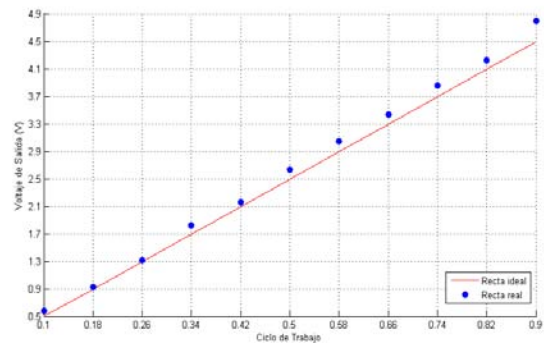

Figure 32. Output voltage of the single-phase converter vs. a variation of duty cycle

The test of the load variation response consists in taking samples of the converter output voltage during a variation of the load demand. At the beginning, there was a high level of noise in the gate. This problem was almost eliminated by removing the gate capacitors and adding one 22nF capacitor connecting the common point to the two MOSFET and to the circuit ground. For this new configuration, the converter output voltage

with a duty cycle of 0.66 was 3.66 V

We connected the load to the single-phase converter, and through the FPGA we gradually altered the values of the load; the results are shown in Table 16. In the graph of Figure 33 we can see the voltage evolution vs. the current.
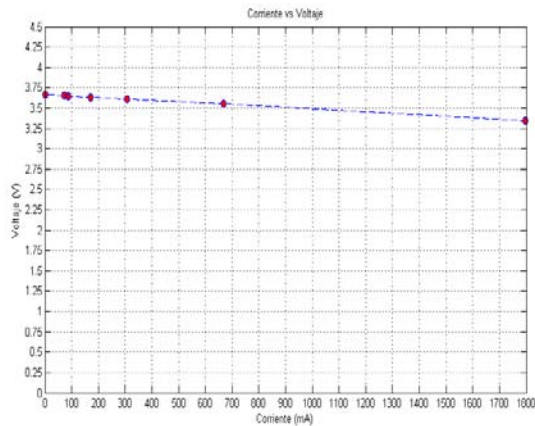

Figure 33. Response to load variation: Voltage vs. current.

The transient test in open-loop transient consists in triggering a drop in the load (an increase in current consumption) and taking samples of the induced change in the output voltage of the converter. For this, as with the previous test, the converter and the load are connected and the oscilloscope is set to perform a single shot.

The test was conducted with a duty cycle of 0.66, and an input voltage of 4.97 V, the drop was made from the burden of 49.96 Ω to 1.7 Ω. In Figure 47 it can be noticed that in the response to this step, the transition takes 29.2 ns and the change is from 3.66 V to 3.35 V through a minimum voltage of 1.94 V.

Figure 34. Response to a Load drop

The final circuit is shown in Figure 35, its main components and the input and output values being marked. The energy flows from right to left through the series inductance Lf and capacitor Cf in parallel to form the input filter, then come the high MOSFET in series and the low MOSFET in parallel, then the main components of the converter which are the inductor Lc in series and parallel capacitor Cc.

The converter control is performed by the FPGA through the IN Low which controls the MOSFET handling the low MOSFET and the input IN High which handles the high-MOSFET.
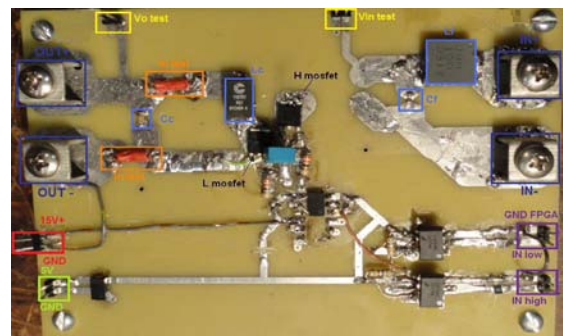

Figure 35. Final circuit of the Multiphase converter

Finally we tested the single-phase converter with the variable load, the A/D converter and the FPGA. With this system, we changed the load through the computer and the FPGA reacts maintaining the output voltage stable.

In the bottom of Figure 37 we can see the feedbacked converter output voltage and the upper part of the figure is the high MOSFET input, we can notice that the controller saturates and goes from 0V to 5V. In Figure 36 we can see the two entries where we can observe that while a switch period is open (3.3 V low active), the other opens and closes. We can also see that the controller reacts to the input signal A/D converter.
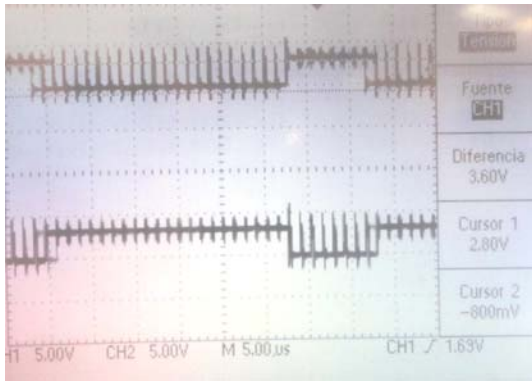
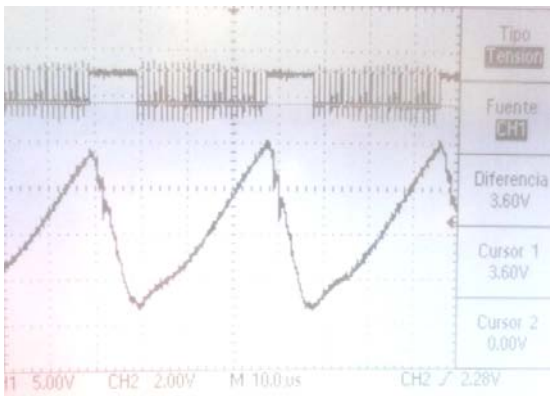Figure 36. FPGA output with the first constants

Figure 37. Voltage output of the converter with the first constants of the FPGA.

In order to improve this response, PID gain was changed until a stable output was obtained. Nevertheless, the 3.3 uF output capacitor was increased by means of putting a 10uF capacitor in parallel, in order to better stabilize the output. In this way the voltage was stabilized at 3.6V.

In Figure 38, the PWM outputs of the FPGA are shown. The switches are activated by low voltage.

Figure 38. FPGA output with the new constants.

Figure 39 shows the output voltage ripple

when the converter is without load and in closed loop. The ripple is 146mV peak to peak which represents a 4.4% of the output voltage.
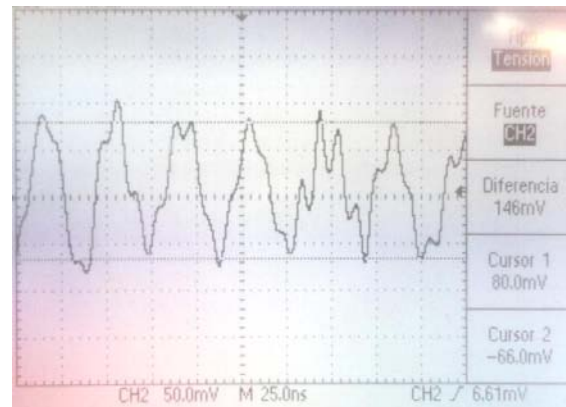

Figure 39. Output voltage ripple of the converter.

V. CONCLUSIONS

Once the project was completed, the single-phase Buck converter and the four A/D converters were put into operation, the dynamic load circuits for two different ranges were ready to use, and the PID control loop was implemented. This loop needs some adjustments in the constants of the control blocks (proportional, derivative and integral) for maintaining the output voltage constant while DC/DC current demand is altered. The platform was tested with the single-phase Buck converter both in closed loop and in open loop, and new algorithms can be tested on it.

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