Real-time noise reduction through independent channel averaging for real-time biomedical signal acquisition

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***Abstract*—In this work, a strategy to obtain a lower noise floor from commercial multichannel Sigma-Delta analog-to-digital converters (ADCs) is presented. Specifically, data from ADS131E08, an 8-channel simultaneous sampling 24 bit converter, is captured, processed, and transmitted in real time using a MAX 10 FPGA included in a measurement system with medical grade isolation, thus able to acquire biomedical signals. Noise measurements show that the system is able to reduce the equivalent input voltage noise of the ADC by a factor of 2.8, extending the measurement dynamic range by 9 dB. In this way, the system improves the otherwise minimum available noise floor with no additional analog stages and allows using higher data rates while maintaining signal quality. Experimental electrocardiogram and electromyogram recordings were taken using non-invasive dry electrodes, validating the operation of the system as a biopotential acquisition platform. Under these experimental conditions, a noise reduction factor of 2.1 times for the noise floor of the measured biopotential signals was verified.**

***Index Terms*—noise, biopotential, average, fpga, sigma-delta converter, dynamic range**

I. Introduction

Sigma-Delta ($\Sigma\Delta$) analog-to-digital converters (ADCs) provide a unique solution for biomedical signal acquisition since their output data stream can achieve a very high dynamic range (DR) and very low noise. When biomedical signals are measured from the body, the transducing electrodes introduce a DC offset with a $V_{off,max} = \pm 300\,\mathrm{mV}$ range. The $V_{off,max}$ value is taken from electrocardiography (ECG) standards for a differential channel [1] and although it is pessimistic, it is often the case that the offset is within a $10\,\mathrm{mV}$ to $100\,\mathrm{mV}$ range. On the other hand, biopotential signals should be measured with a noise floor on the order of $1\,\mu\mathrm{V_{rms}}$ or less [2], [3] which can be translated to a signal amplitude of $6\,\mu\mathrm{V_{pp}}$ considering $\pm 3\sigma$ thus taking the dynamic range to $20\log_{10}(600\,\mathrm{mV}/6\,\mu\mathrm{V}) = 100\,\mathrm{dB}$.

If high-pass filtering is applied the dynamic range is reduced by blocking the DC offset decreasing the necessary DR to the approximately 70 dB needed by the signal itself. In these cases, the usual strategy is to apply filtering in combination with a relatively high amplification factor to allow acquisition with a $12\,\mathrm{bit}$ to $14\,\mathrm{bit}$ ADC. However, there are a number of disadvantages to this methodology. The first disadvantage is simply the necessity of an analog stage capable of providing a relatively high gain in the order of 100-1000 times while rejecting DC electrode offset components [4]. The second is related to a form of interference affecting biomedical measurements called *artifacts* which are produced when the electrodes or the skin are mechanically perturbed (e.g. by pulling the cables or by the displacement of the muscles themselves). Artifacts produce wide fluctuations of the baseline signal which can saturate filters and amplification stages, that in turn may take a long time to return to an operational range. Moreover, front-end solutions with additional amplification may require further complex balancing circuits [5] compared with unity-gain solutions [6].

Thus, high dynamic range, low noise $\Sigma\Delta$ converters have been identified as advantageous for biomedical signal measurements [7] and this strategy is incorporated in state-of-the-art integrated acquisition systems [8], [9]. The semiconductor industry has included these ADCs in commercial application-specific standard products (ASSPs) such as the ADS129x and ADS13x lines from Texas Instruments and AD7779 from Analog Devices, as some examples. These ASSPs are useful in programmable-logic-based systems as biomedical signal front-ends [10], [11].

Sigma-Delta converters are among the highest DR ADCs commercially available and achieve a very low referred-to-the-input (RTI) noise voltage. The RTI noise is in fact sufficiently low to enable biomedical signals to be acquired with no amplification, preserving the full DR of the device. However, augmenting the output data rate (ODR) results in a degradation of the noise properties of these devices because of their fundamental trade-off between resolution and bandwidth [12]. This trade-off can be seen in Table I, where values obtained from Table 1 and Equation 1 of ADS131E08's datasheet [13] are displayed. The motivation of the presented work is to further extend the capabilities of commercial $\Sigma\Delta$ ADC devices making (i) previously unavailable noise-floor levels feasible without additional analog stages and (ii) lower noise levels at

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TABLE I: ADS131E08 specifications parametrized by gain and output data rate (from its datasheet [13])

Gain - ODR*	1 - 1 kHz	12 - 1 kHz	1 - 16 kHz	12 - 16 kHz
DR [dB]	117.7	108.0	102.8	94.2
ENOB † [bits]	19.6	18.0	17.07	15.65
RTI N. ‡ [μV_{rms}]	2.13	0.54	12.33	2.75

*Output Data Rate.
† Effective number of bits.
‡ Referred-to-the-input noise voltage.

higher data rates available.

II. Method

A. Signal-to-noise ratio improvement through averaging

One strategy to improve the signal-to-noise ratio (SNR) of an ADC is to use oversampling by which temporal averaging is used to reduce noise. However, this technique implies a reduction of the ODR. If several independent ADC channels are available, the SNR can be improved by simultaneously acquiring the same signal with all channels and then averaging across all digitized samples [14], [15] as shown in Fig. 1.

Considering a signal $v_{in}(t)$ which is sampled obtaining

$$x(k) = v_{in}(kT) + n_{ADC}(k) = s(k) + n_{ADC}(k) \quad (1)$$

where n_{ADC} is the noise introduced by the analog-to-digital conversion process and $s(k)$ is the sampled signal of interest, the output of the N-channel averaging stage is equal to

$$y(k) = \frac{1}{N}\sum_{i=1}^{N} x_i(k). \quad (2)$$

After applying (2) to the N input signals given by (1) then

$$\begin{aligned} y(k) &= \frac{1}{N}\sum_{i=1}^{N}\left(s_i(k) + n_{ADC,i}(k)\right) \\ &= s(k) + \frac{1}{N}\sum_{i=1}^{N} n_{ADC,i}(k) = s(k) + n_T(k) \end{aligned} \quad (3)$$

The output $y(k)$ contains the unmodified component of the signal of interest $s(k)$ and the averaged noise from all channels $n_T(k)$. While for ideal ADCs quantization noise is linked to the weight of the least significant bit (LSB), the noise contribution of $\Sigma\Delta$ converters is measured by an equivalent number of bits (ENOB) which corresponds to the root mean square (rms) noise level and is dependent on the output data-rate and the digital filter implementation.

Given the assumption that the noise is an independent identically distributed (iid) random process with Gaussian distribution, the rms value can be obtained by calculating its standard deviation σ_{ADC}, which can then be further estimated by the standard deviation over sampled time k under the assumption of ergodicity.

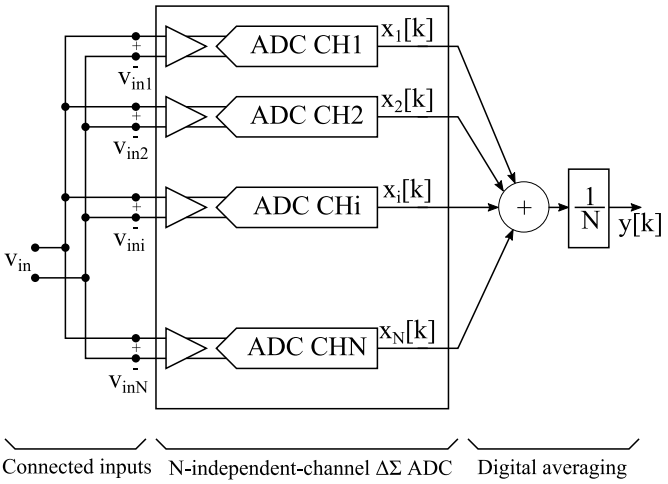

Fig. 1: Block diagram of the simultaneous sampling averaging scheme.

The total noise component present in the output signal will have a variance given at each instant k by

$$\begin{aligned} E\{n_T(k)^2\} = \sigma_T^2 &= E\left\{\left(\frac{1}{N}\sum_{i=1}^{N} n_{ADC,i}\right)^2\right\} \\ &= \frac{1}{N^2}\sum_{i=1}^{N}\sigma_{ADC}^2 + \frac{1}{N^2}\sum_{i=1}^{N}\sum_{j=1}^{N,i\neq j}\rho_{i,j}\sigma_i\sigma_j \end{aligned} \quad (4)$$

Where $\rho_{i,j}$ is the correlation between the noise of pairs of channels and $E\{n_{ADC,i}\}$ has been considered 0. The best case is given if all channels are uncorrelated and hence $\rho_{i,j} = 0\,\forall\, i \neq j$ therefore

$$\sigma_T^2 = \sigma_{ADC}^2/N \;\; \therefore \sigma_T = \sigma_{ADC}/\sqrt{N} \quad (5)$$

yielding a SNR improvement equal to $\sqrt{N}$ [14], [16]. The worst case is given when the correlation between all noise signals is 1 in which case $\sigma_T = \sigma_{ADC}$ and the SNR is exactly the same as if no averaging had been performed.

B. System implementation

An acquisition system was built in order to capture data from an ADS131E08 ADC and perform the average of its channels per (2). The system was implemented as a full biopotential acquisition platform including medical grade isolation in order to perform biopotential measurements. Its main blocks and their interconnections can be seen in Fig. 2.

The ADS131E08 has 8 independent $\Sigma\Delta$ ADCs, each with a programmable gain amplifier (PGA). The 8 channels perform simultaneous sampling of each of their differential inputs. The output data rate is configurable from 1 kHz to 16 kHz. Higher 32 kHz and 64 kHz data rates are available but the dynamic range is reduced to less than 16 bits, therefore they were not used.

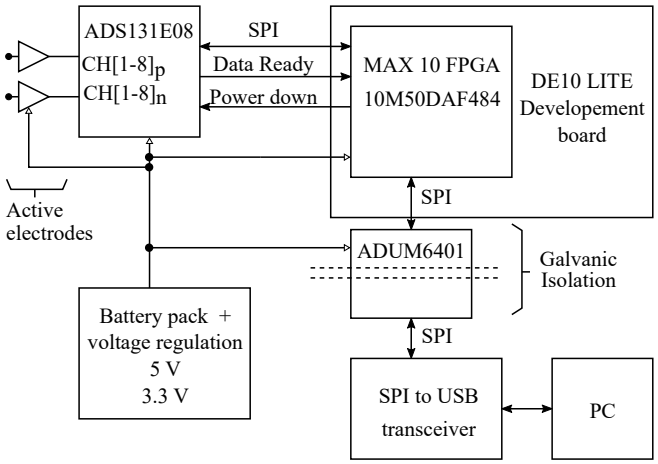

Fig. 2: Block diagram of the biopotential acquisition system implementation.

The core element controlling the system is a MAX 10 10M50DAF484C7G FPGA from Intel (previously Altera) used in a DE10 LITE development board from Terasic. The rationale for selecting an FPGA instead of a microcontroller platform was that for the latter the volume and rate of data can represent a demanding task. In contrast, an FPGA would be scarcely demanded (as will be shown later in this work) and has the potential to further develop both the technique by including more complex processing, and the acquisition platform by including user and data interface capabilities.

The system was configured with a set of finite state machines (FSMs) controlling a communications interface to program ADS131 registers and receive its data output, summing logic to perform the average, and a second communications interface to send the data in real time to a personal computer (PC). The ADS131 interface consists of a master serial peripheral interface (SPI) bus plus control lines required by the converter. The interface with the PC is achieved through a second master SPI bus sending the processed output data in a frame for serialized transmission. The behavior and function of the configured FSMs are shown in Fig. 3. A $50\,\mathrm{MHz}$ clock included in the DE10 Lite board was used as input to a phase-locked loop (PLL) to obtain a $100\,\mathrm{MHz}$ master clock signal. The SPI master module was sourced from OpenCores SPI MASTER/SLAVE project [17].

C. Experimental setup

In order to ascertain the viable noise reduction that can be obtained with the proposed technique, all channels of the ADS131E08 ADC were short-circuited to a voltage reference using the internal multiplexer of the device. The resulting RTI noise was evaluated by taking $32\,000$ samples at $1\,\mathrm{kHz}$ and $16\,\mathrm{kHz}$ for all available gains (1, 2, 4, 8 and 12), and at gains 1 and 12 for all available output data rates (1, 2, 4, 8 and 16 kHz). Results were compared with data extracted from Table 1 and Equation 1 of ADS131E08's datasheet [13].

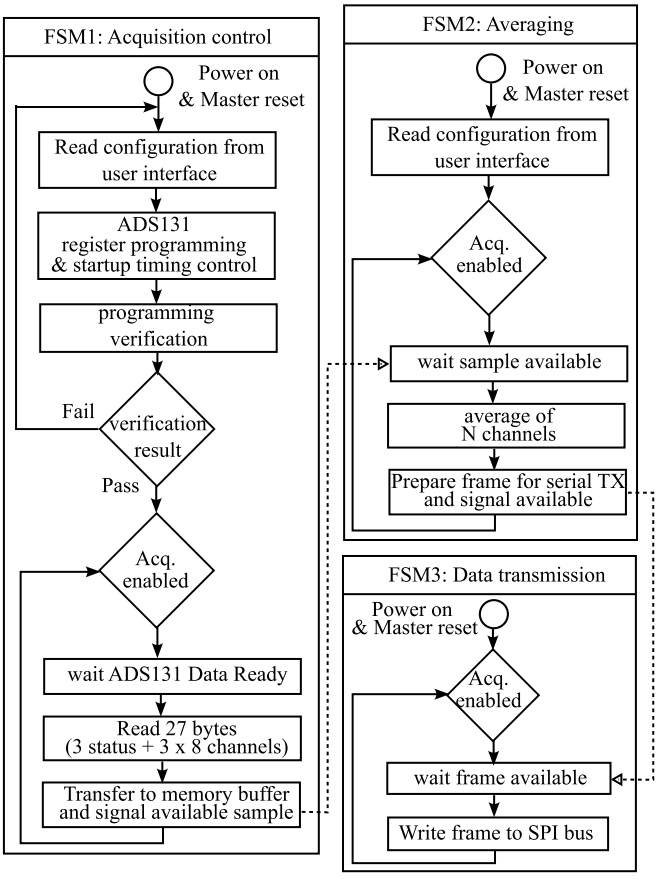

Fig. 3: Programmable-logic system configuration.

Biopotential measurements were carried out to validate the usefulness of the acquisition system and noise-reduction impact. A previously reported driven-right-leg (DRL) independent electrode [18] was connected to the isolated power provided by the board with a reference of $1.2\,\mathrm{V}$. Measurements were performed by attaching two active electrodes composed of operational amplifiers (OAs) in unity-gain buffer configuration to the positive and negative inputs of the ADS131 ADC respectively. Therefore, one differential channel can be measured with the active electrodes shown in Fig. 2 and routed to v_{in} signal shown in more detail in Fig. 1, thereby connecting it to the 8 inputs simultaneously. The buffers in the active electrodes serve to mitigate electromagnetic interference (EMI) due to capacitance couplings to the wires as is their usual function [19] and in this case, are paramount to avoid input impedance degradation due to the connection to multiple input stages in parallel.

III. Results

A. System implementation

The implemented acquisition system is shown in Fig. 4 with the blocks from Fig. 2 marked with text commentary. The

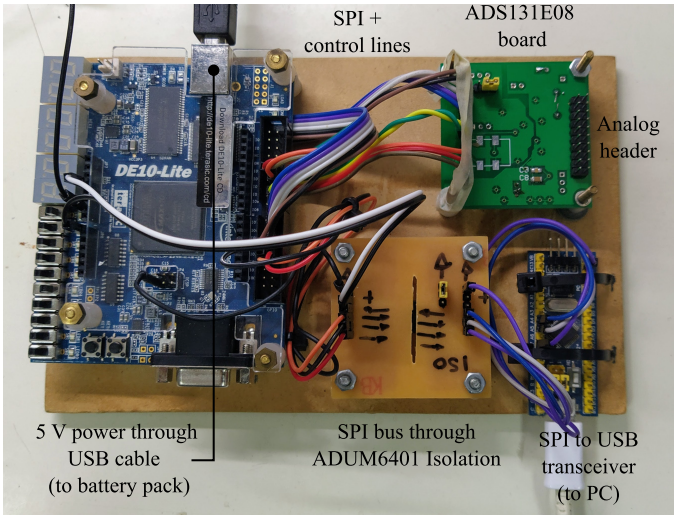

Fig. 4: Photograph of the acquisition system.

Resource utilization	
Total logic elements	1,845 / 49,760 (4 %)
Total registers	1446
Total memory bits	640 / 1,677,312 (<1 %)
Total PLLs	1 / 4 (25 %)
Timing Analysis	
Maximum Frequency	125.2 MHz

TABLE II: Implementation details for 10M50DAF484C7G device.

summary of the total utilized resources of the programmable-logic device is shown in table II. The timing results were obtained with the Timing Analyzer tool from Intel's Quartus Prime software, for a 1200 mV 85C model.

B. Noise measurements

Noise measurement results are sown in Fig. 5 and Fig. 6.

In Fig. 5 two sets of values of the measured RTI noise are shown joined by a full line: they correspond to the noise of one channel at 1 kHz and 16 kHz ODRs for its 5 gain configurations. A higher gain results in lower RTI noise since the contribution of stages after the programmable gain amplifier has less weight. The effective noise reported in the component's datasheet is shown in small dots and it coincides up to within a 5 % with all measurements except the 16 kHz, 12x gain which consistently deviated with a 13 % lesser noise. In the same figure, the results of the averaged measurements are shown in dashed line, verifying that a noise reduction was indeed obtained. At a 1 kHz data rate, noise was reduced by a factor of 2.9 ± 0.1, and at 16 kHz by 2.97 ± 0.08.

Noise measurements from the lower and higher gain configurations (1 and 12) are further shown in Fig. 6, again joined by a full line for the RTI noise of the single-channel case, with markers at the 5 data rate configurations and small point markers showing the component's datasheet values. An average noise reduction of 2.80 ± 0.05 was obtained for gain 1, and 3.04 ± 0.02 for gain 12.

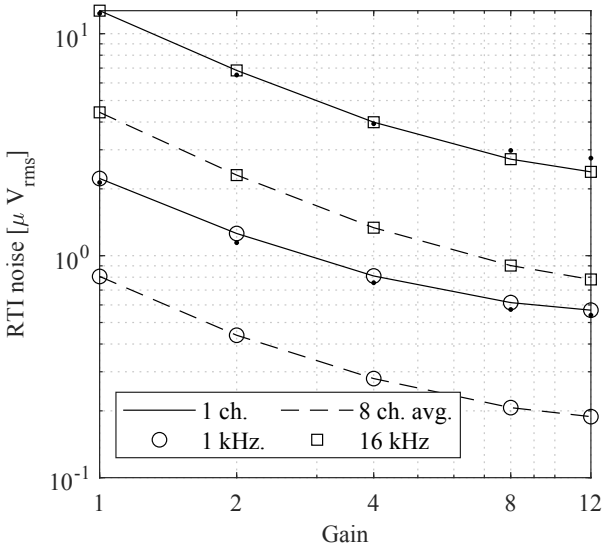

Fig. 5: Measured RTI noise for 1 kHz and 16 kHz data rates at different gain configurations. The full line follows measurements of a single channel and the dashed line the 8 channels averaged.

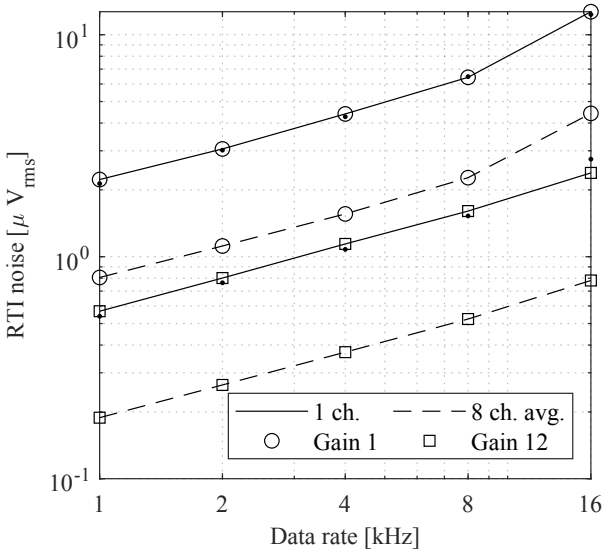

Fig. 6: Measured RTI noise for gain of 1 and 12 at different data-rate configurations. The full line follows measurements of a single channel and the dashed line the 8 channels averaged.

The results from Fig. 5 and Fig. 6 show that for ADS131E08 it is possible to reduce noise by channel averaging. The reduction factor is slightly higher than the expected for the 8-channel average ($\sqrt{8} = 2.82$) and could be explained by a deviation from the simplified statistical assumptions made, and the necessary use of an estimation of the standard deviation. However, it is an indicator that there are no inter-channel correlations preventing noise reduction. The lowest measured reduction coincides with the theoretical value, and it effectively extends the dynamic range by 9 dB.

The absolute noise levels obtained by averaging show that for biomedical signal measurement applications, no additional amplification circuit would be needed at a frequency as high as $16\,\mathrm{kHz}$ to attain $1\,\mu\mathrm{V_{rms}}$, since all values for a gain of 12 are below this limit. Moreover, a gain of 8 is sufficient to achieve the target noise level at the $16\,\mathrm{kHz}$ rate. This is significant since this data rate allows acquiring fast spike potentials with a $4\,\mathrm{kHz}$ bandwidth present in invasive measurements [20]. The $9\,\mathrm{dB}$ DR extension for the fastest data rate takes the DR to $103\,\mathrm{dB}$ again above the desired values. On the other hand, the low noise levels achieved on the lowest frequency settings, for example, $0.19\,\mu\mathrm{V_{rms}}$ for a $1\,\mathrm{kHz}$ ODR at gain 12 while preserving a $117\,\mathrm{dB}$ DR, can be useful for electroencephalography (EEG) measurements which present challenging low-noise requirements [2] and in some cases benefit from DC-coupled acquisition [21].

C. Biopotential measurements

In order to validate the operation of the system for real-time biopotential acquisition, a set of in-vivo measurements were performed.

First, an electrocardiogram (ECG) recording was taken using a differential channel with active electrodes implemented with OPA378 operational amplifiers (OAs) in buffer configuration (gain of 1). Two standard adhesive wet Ag/AgCl electrodes were placed frontally below the thorax and the DRL on the waist. The system was configured with an output data rate of $1\,\mathrm{kHz}$ and gain of 1. Measurements were taken 10 minutes after attaching the electrodes. The channel averaging was first turned off producing the upper line from Fig. 7, and then it was activated to perform the 8-channel average. The result is shown in the lower trace of Fig. 7. In this case, the noise floor was imposed by the measurement electrodes, and the signals show a match validating the averaged configuration acquisition capability.

Next, electromyography (EMG) measurements were conducted by placing two dry electrodes on the forearm, affixed with an elastic fabric band, and performing finger contractions. The system was configured with a $16\,\mathrm{kHz}$ output data rate and gain of 1. Fig. 8 shows the measurement results. A very slight contraction was performed between seconds 0 and 2, and a stronger contraction between seconds 5 and 8. An effort to relax the muscles was instructed between these two contractions, and within these segments the noise reduction is observable despite the presence of the base noise floor of the dry electrodes. In order to observe the properties of the system, different passband filters were applied in Fig. 8a and 8b. In 8a a low-pass frequency of $4\,\mathrm{kHz}$ was used and the noise reduction obtained with averaging is seen by inspection, with a reduction factor of 2.1. Under these conditions, the activity resulting from weaker contractions is not observable. In Fig. 8b, standard band-pass filtering for superficial EMG was used [3] and the signal quality improves, with a reduction gained by averaging of 1.12. The bandwidth used in Fig. 8a is excessive for superficial EMG but would be useful in invasive EMG or electroneurography (ENG) measurements where the full bandwidth of biopotential spikes up to $10\,\mathrm{kHz}$ can be acquired [20].

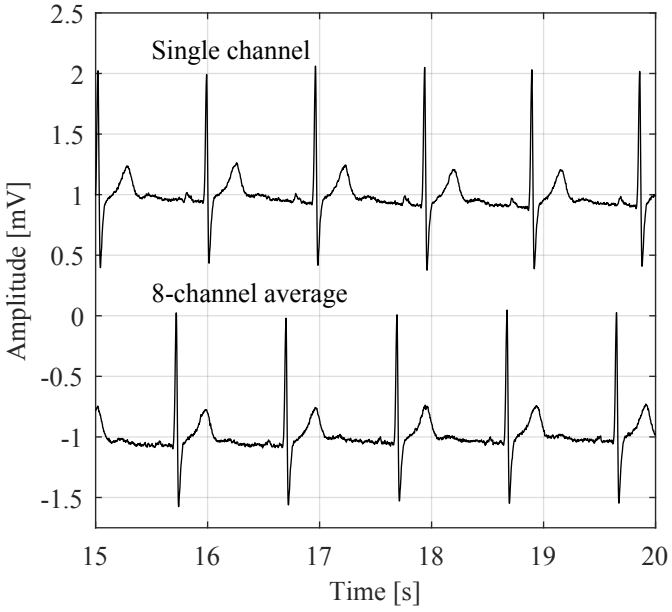

Fig. 7: Recording from ECG measurements.

IV. Conclusions

Noise reduction through the averaging of $N = 8$ channels of a simultaneous sampling high-resolution Delta-Sigma analog-to-digital converter was shown to be feasible and in the order of the theoretical reduction for independent identically distributed noise sources, $\sqrt{N}$. The capabilities of the implemented system for real-time biomedical signal acquisition and processing were demonstrated by a set of ECG and EMG in-vivo recordings.

Considering the recommended noise floor for biomedical signal acquisition, the application of this method for ADS131E08 $\Sigma\Delta$ ADC allows measuring with no additional analog amplification besides the integrated programmable-gain-amplifier for data rates of $4\,\mathrm{kHz}$ to $16\,\mathrm{kHz}$, using a gain setting of 12. Further, acquisition with a configuration of $1\,\mathrm{kHz}$ data rate and gain of 1 is possible thus preserving the full available dynamic range. In addition, the lowest noise floor (for $1\,\mathrm{kHz}$ data rate and gain of 12) was reduced to $0.18\,\mu\mathrm{V_{rms}}$.

The presented method allowed reducing the equivalent input voltage noise of the ADC by a factor of 2.8, extending the measurement dynamic range by 9 dB. This technique can thus be useful to reduce the noise floor in measurements using $\Sigma\Delta$ converters with no additional analog stages and to achieve higher data rates without sacrificing signal quality.

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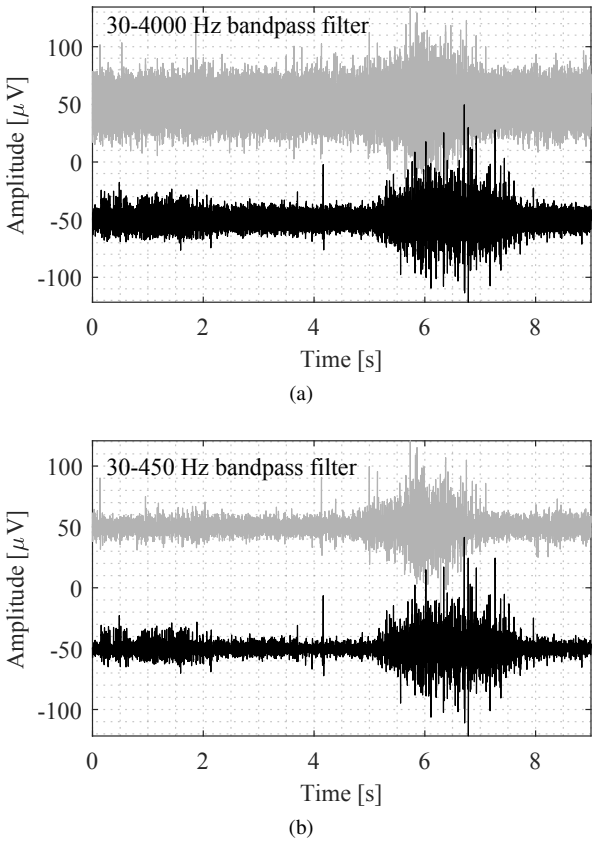

Fig. 8: Superficial EMG measurement recordings. The gray line marks a single-channel measurement and the black line marks a measurement performed using averaging. (a) and (b) have different pass-band filters applied as described in the text.

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