An Implementation on FPGA For a Time Base Corrector

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ABSTRACT

The main motivation of this work arose while working on video restoration with old and valuable playback systems but with misalignment between record and playback heads.

Brand new systems include systems like the one shown here. This solution aims to solve in a practical and cheap way problems in old but still usable VCR systems to be used as a source for digital restoration.

Hereafter an implementation over FPGA of a well documented solution for the digital time base distortion that usually affects magnetic tape recorders for audio and video is presented.

A brief explanation about the blocks involved is given as well as a further discussion about the ideas considered to implement the overall design.

1. INTRODUCTION

Re-using old film and video material is only feasible if the visual and audio quality meets the standards expected by the modern viewer.

If one considers that archived film and video sequences will be preserved by transferring them onto new digital media, there are a number of reasons why these sequences should be restored before renewed storage. First, restoration improves the subjective quality of the film and video sequences (and thereby increases the commercial value of the film and video documents). Second, restoration usually leads to more efficient compression, i.e., to better quality at identical bitrates, or, conversely, to identical quality at lower bitrates. The latter is especially important in digital broadcasting and storage environments for which the price of broadcasting/storage is directly related to the number of bits being broadcast/stored.

The most important step for restoration is starting from a perfect, skew-free, video signal and here is where the time base corrector (TBC) plays a main role. [Pra91], [Mul96], [Ban97]

The purpose of the TBC is to strip the video signal of its damaged timing and insert a new, clean timing. This will remove many motion errors, such as jittering video and brightening/darkening of the image.

Time base distortion occurs whenever a signal, or a portion thereof, occurs too early or too late relative to a reference time frame. In a multi-channel longitudinal recorder, a multi-channel recording head is used to record information signals along a plurality of tracks on a recording medium such as a magnetic tape. The recorded signals are played back by means of a multi-channel playback head.

If the recording and playback are perfectly aligned, and if the transport system that advances the recording medium does so at a perfectly uniform velocity, the played back signals represent a faithful reproduction of the originally recorded information signals. Practical systems, however, are not so perfect.

A conventional multi-channel magnetic (recording or playback) head has a stack of aligned transducer gaps. The alignment of such gaps constitutes a "gap line". *The recording and playback heads are perfectly aligned when the respective gap lines have the same azimuthal angle (e.g. 90 degrees) with respect to the direction of tape advancement*. For various reasons, however, the recording and playback heads in practical systems are often not perfectly aligned. Such misalignment has the effect

of producing time base distortion in the form of relative phase errors among the played back information signals.
The solution provided here, is an adaptation for its implementation on FPGA of that presented on early 80's by Colles et al [Col82]. Other ideas were considered [Wag97] but the one that best provided the features searched for this design (simplicity and economy) was that of Colles.

2. CIRCUIT BASICS

To apply time base correction, a time base error generator generates a time base correction factor to be applied to the signal stored in the RAM. An analog to digital converter (ADC) encodes the time base correction factor to an 8-bit digital word that is applied to a programmable read-only memory (PROM). The four output lines O_4 through O_7 from the PROM are connected to the least significant load inputs (L_1 through L_4) of the read address counter, thereby determining the initial count at which the read address counter addresses the RAM. The PROM is programmed such that the load input to the read address counter causes the counter to skip as many storage cells as necessary (up to 16) to correct for time base error to within one cycle of the counter clocking signal.
In general, however, the time base correction factor will not always be a whole number of clock cycles. For example, it may be desired to delay the signal by a time corresponding to $3_{1/8}$ clock cycles. To provide such sub-cycle accuracy, the four output lines O_0 through O_3 of the PROM are used to address a 1 of 16 data selector.
Fig. 1 shows the general structure of the blocks involved in the model explained above as presented in [Col82].

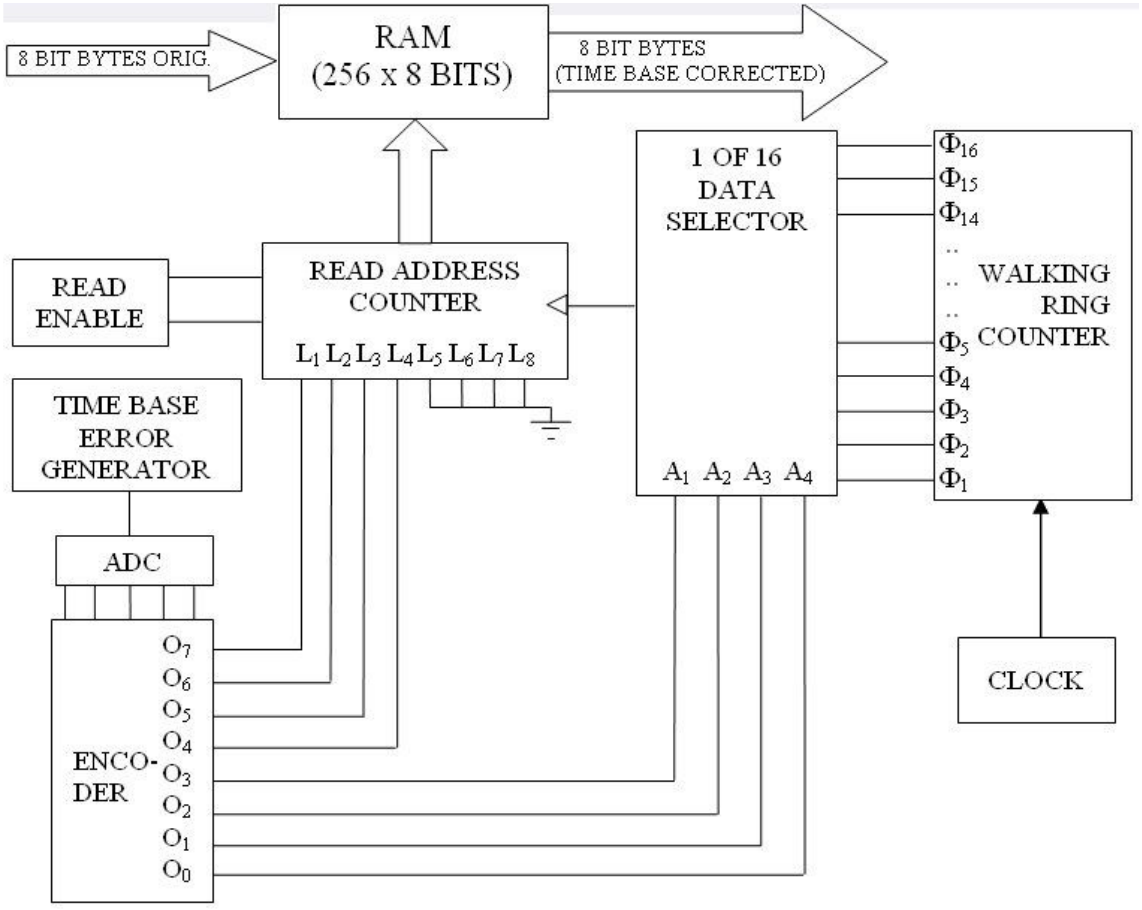

Fig. 1 – Schematic blocks diagram

Summarizing, this circuit receives the signal to process digitized as a byte stream stored in the RAM, and the time base corrector provides a suitable set of clock phases (within one-sixteenth of a clock cycle) to correct skew distortion.
The new generated signal is stored once again in the RAM (which acts as a buffer) from where is provided to the interface output system.

Fig. 2 shows the relationship between information in the timing signal and information in the video signal.
It's worth to point out that this paper doesn't aim to provide an exhaustive level of detail regarding the implementation but the main general idea of using programmable devices for prototyping (and implementing) feasible solutions in the field of video restoration.

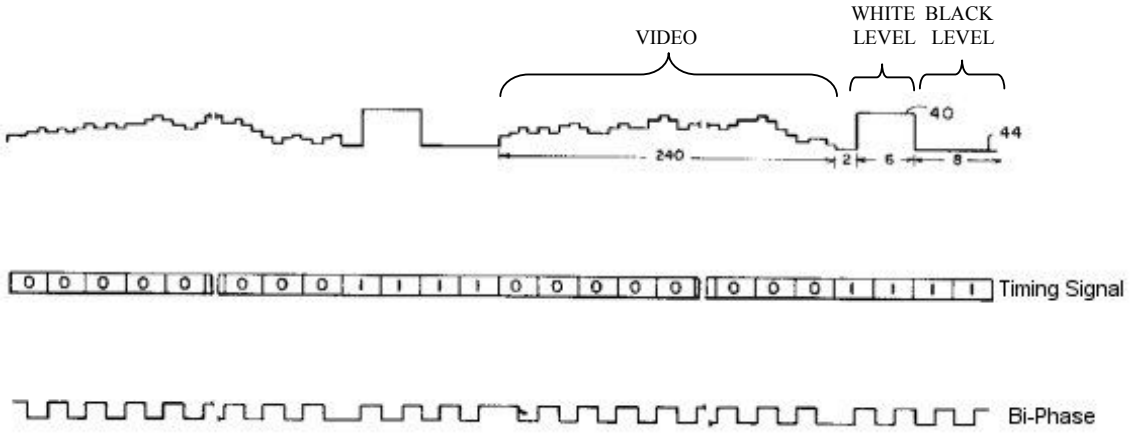

Fig. 2 – Timing signal and video signal

3. CONCLUSIONS

All blocks are to be implemented on VHDL and synthesized by means of Xilinx ISE to target a XC2S200E device [Xil03]. All preliminary tests and timing diagrams obtained though simulation were successful. Once the full circuit board (involving TBC and interfaces) is finished, testing will be achieved through a montage as shown in Fig. 3.

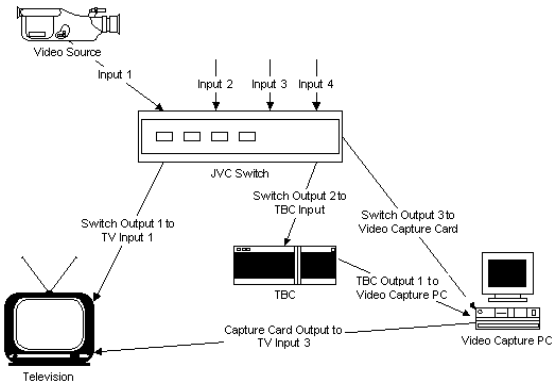

Fig. 3 – Test bench for the TBC

Video source to be used is a JVC HR-S9800U deck with a video tape containing a TV program recorded to S-VHS master-quality tape. The video switch is a JVC JX-S700 and the PC's capture card is a Pinnacle DC1000.
This implementation is intended as a starting point for a further signal restoration tool set to be integrated in the same programmable devices where each functionality is provided as customizable cores.
Examples of such modules for impairing old film and video sequences might include hardware tools for avoiding defects in these signals, i.e. noise, blotches, line scratches, film unsteadiness and intensity flicker.

4. REFERENCES

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