Multilevel Current Source Inverter to Improve Power Quality in a Distribution Network

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Abstract – **This paper deals with the problem of reactive power and harmonics in a standard medium voltage (MV) distribution network. It presents the design of a shunt active filter implemented with a multilevel current source inverter (MCSI) connected to the medium voltage level of a power distribution system. The proposed MCSI is made by identical modules where all inductors carry the same amount of current. The current balance is achieved by a Phase-Shifted Carrier SPWM proper implementation. The performance of proposed active filter is thoroughly simulated with Matlab Simulink. It shows very good behavior in steady state and transient conditions.**

I. INTRODUCTION

Power quality in distribution systems is seriously affected by harmonics introduced by the loads. Power factor is another issue to deal with when maximum efficiency of the system is pursued. Both problems can be solved in a medium voltage distribution system by adding a shunt active filter based on a Multilevel Current Source Inverter (MCSI).

Multilevel voltage source inverters (MVSI) have been used in power factor correction and active filters applications in recent years [1], but they require high voltage and high ripple current capacitors [2] whose life spam and stability are worst than those for inductors, leading to a higher failure ratio. Inductors might be less volume effective than capacitors but they have a much longer cycle life. They can stand high voltage ripple without losing performance and their electrical attributes hardly change with time, as long as good power dissipation is provided. This means higher reliability, larger mean time between faults (MTBF) and less maintenance needs. Inductors built with high temperature superconductors will reduce losses, turning MCSI into the most efficient solution for multilevel inverters [3].

Multilevel topologies present several advantages in both VSI and CSI structures, regarding total harmonic distortion and stress on components and switches [2] [4]. Nevertheless they have not yet been widely applied, the MCSI appears as a smart choice to improve performance and efficiency in medium voltage distribution systems and industrial applications where high power or high current are required, such as active filters, motor drives and HVDC [5].

In this paper a single-rating-inductor-MCSI is employed to implement an active filter [6]. The converter consists of three identical modules which generate seven current levels [7]. Each module uses two balance inductors and six power switches. Both inductors of every module should carry the same current. The current flowing through the inductors can be balanced when applying a state machine modulation that properly uses the redundant zero states [8][9]. Moreover the switching frequency can be reduced with this modulation. The modulation and gate drives control logic are implemented on a Field-Programmable-Gate-Array (FPGA) [10], which is a powerful, cost-effective solution. It allows complex logic and control algorithms, fast speed and multiple I/O pins, which becomes especially attractive for multilevel converters control.

Fault tolerant assembles are easy to develop and operate because all modules are identical. Fault tolerant capabilities are a mayor feature in power quality increasing reliability and reducing MTBF. They can be achieved by adding hot spare modules and have been already demonstrated for the converter in [11].

This paper presents a simple approach, showing that a good power factor correction performance and harmonic current minimization can be provided. Current balance among modules is sustained by adapting a well known PWM strategy [9] while minimizing switching speed using a sequential machine approach. In detail, the paper is organized as follows. The system is described in Section II. The active filter is analyzed in Section III, including a comprehensive analysis of the inverter in section III A and the control scheme in section III B. The performance of the proposed filter is evaluated in section IV with simulations. Finally, some conclusions are drawn in Section V.

II. SYSTEM DESCRIPTION

The one line diagram of the system model adopted for the medium power distribution system under test is shown in Fig.1. The loads of the different substations are mainly commercial and residential, so it is more difficult to identify the harmonic sources than in the case of industrial plants. Then, it is necessary to build a model based on the field measurements [12].

The system is represented as an ideal voltage source of 132 kV connected to three transformers of similar characteristics, 132/34.5/13.8 kV and 15/10/15 MVA. The system is modeled by its equivalent impedance related to

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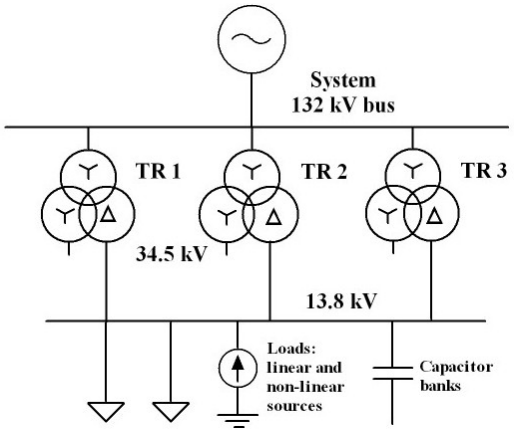

Fig. 1. One line diagram of system model.

short circuit power at 13.8 kV. There are no loads at the 34.5kV level. All transformers are connected in parallel to 13.8kV where the loads are placed. Due to the transformer windings connection, Wye/Wye/Delta (Y/Y/D), there is no zero sequence register at 13.8 kV level.

The measurements performed on the network have shown that the load currents present no negative sequence fundamental component. Then, a balance model network is built for the system under study [12].

The active and reactive power demand at the fundamental frequency is represented by a constant impedance model. The non-linear load, corresponding to harmonics, is modeled with sinusoidal current sources. Their amplitude and frequency match those of each harmonic measured in the system. Based on the power flow and harmonics studies performed on the system, the power total demand at the 13.8kV bus is 30 MVA with a cos φ = 0.8. The harmonic peak currents and the THD_I, considering up to the 50th harmonic, are shown in Table I.

Table II summarizes the harmonic voltages and THD_V with the limits fixed by IEEE [13]. The individual harmonic voltages for the 5th, 7th, 11th and 13th harmonics and THD_V are above the allowable levels (Fig. 2), so reactive and harmonic compensation must be considered.

The target of the proposed compensator is to obtain cos φ = 0.96 at 13.8kV level. Then, 11 MVAr will be required to the inverter [14]-[16].

TABLE I
HARMONIC CURRENTS

i_h	i_5 (A)	i_7 (A)	i_{11} (A)	i_{13} (A)	THD_I (%)
Peak values	81.6	58	37.2	31.4	5.45

TABLE II
HARMONIC VOLTAGES

Harmonic Voltages	100 % load	IEEE limits
V_5 (%)	**3.07**	3
V_7 (%)	**3.04**	3
V_{11} (%)	**3.05**	3
V_{13} (%)	**3.04**	3
THD_V (%)	**6.10**	5

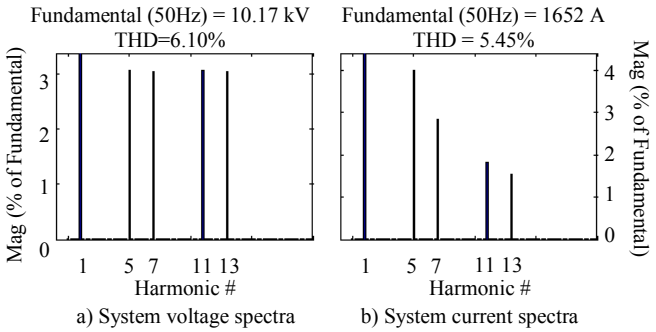

Fig. 2. System voltage and current spectra without compensation

III. ACTIVE FILTER

The active filter consists of a Multilevel Current Source Inverter connected to the grid with small filtering capacitors to avoid over voltages due to current transitions (Fig. 3). A ripple filter is added to derive the high frequencies generated by the inverter. The current references for the MCSI are generated by the control block developed in a rotating reference frame (dq0), synchronous with the positive sequence of the system voltage [1].

The main current source of the inverter (dc side) consists of one inductor of proper value whose current can be regulated exchanging active power with the system.

The output capacitors of the inverter only drain 478kVAr which is a small portion of the total reactive power. Their capacitance is calculated to avoid that the resonant frequencies of the system match the harmonics generated by the converter.

The analysis of the active filter is divided in two sections: the MCSI, and the control block to obtain the desired behavior.

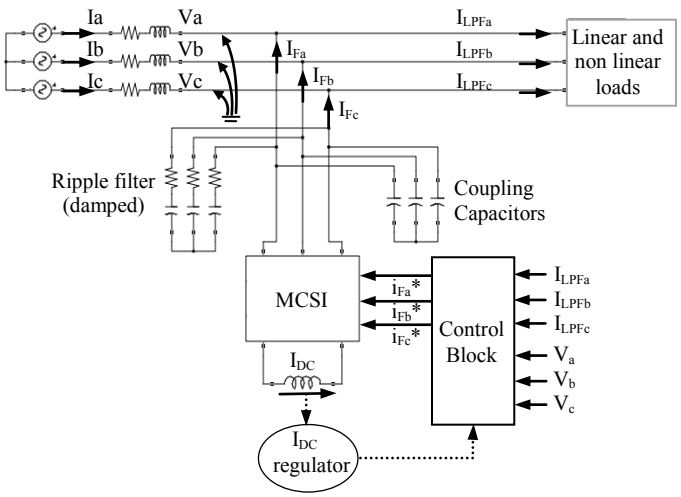

Fig. 3. General structure of the active filter

A. *Multilevel Current Source Inverter*

Several Multilevel-CSI topologies have been developed, e.g. multi-rating inductor, cascade H-bridge and single-rating inductor. Multi-rating-inductor-MCSI requires only two balance inductors for two adjacent modules but every pair of balance inductors carries different current values. There are no balance inductors in the paralleled H-bridge-MCSI although the use of multiple independent dc current sources is necessary [6].

The converter topology presented in Fig. 4, also known as "single-rating inductor MCSI" [6], consists of multiple CSI sub circuits, connected in parallel with the system, and sharing a common current source. Each group of six switches and two inductors will be referred as a *module*. Those *sharing inductors* split in equal shares the current from the main source.

The major advantage of this MCSI configuration is its modular structure, where each identical module handles only a fraction of the load current [6][11]. The number of levels in the output current can be determined according to the number of modules,

$$i_n = \frac{m-n}{m} I_{DC} \qquad n=0,1,\ldots,2m \tag{1}$$

where m represents the number of modules and n goes from 0 to $2m$. In this paper we consider m=3 to obtain seven levels of load current,

$$\frac{i_l}{I_{DC}} = \left\{1,\ \frac{2}{3},\ \frac{1}{3},\ 0,\ -\frac{1}{3},\ -\frac{2}{3},\ -1\right\} \tag{2}$$

The proposed inverter uses eighteen identical switches with bidirectional blocking capability. They are implemented with IGBT transistors and diodes in series connection. The voltage and current levels proposed in this paper can be achieved with present IGBT technology [17].

Different load current levels can be obtained by turning on or off each switch. As in many multilevel topologies each output current level can be generated by more than one combination of switches. For example, closing switches A6, C5 and B6 would have the same effect of closing A5, B6 and C6. This redundancy gives some degree of freedom to work on the current balance of all inductors and to minimize the switching frequency of the converter.

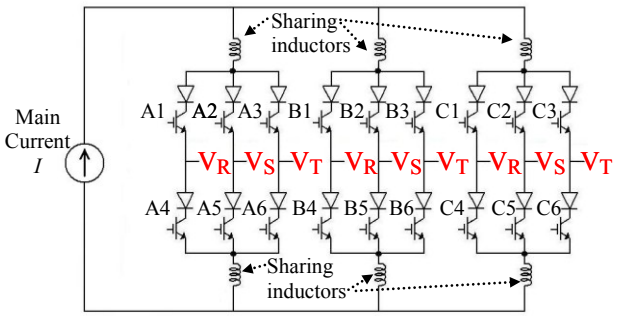

Fig. 4. Basic Multilevel CSI scheme.

The control of the whole converter is based on the individual control of each module with sinusoidal PWM and the use of Phase Shifted Carriers in the modulation of the different modules to guarantee the current balance in all the inductors [18].

In a standard SPWM configuration for Voltage Source Inverters the switches on a single branch are turned on or off depending on whether the control signal is greater or smaller than the carrier. But in order to guarantee that the current of the module is imposed to a certain phase of the load, the actual driving signals are obtained with some manipulation of the signals produced by a standard SPWM as shown in [11].

Firing signals generated by the SPWM logic cannot directly drive IGBT's gates since they generate zero states by turning off all switches. This does not allow inductor's current continuity in a CSI. Zero states generated by the SPWM logic should be recognized and replaced by adequate ones.

Each CSI module can generate zero states in seven different ways. Correct zero state implementation is mandatory to minimize the number of switching transitions per fundamental cycle for each switch thus lowering the power dissipation. A logic state machine allows to select the optimal zero combination. The active states are not affected by the state machine and pass through it unchanged. As an example of the effect of the sequential machine on commutation of the power switches the gate signal of switch A1 is shown in Fig. 5. Gate signals generated with the state machine zero selection (Fig. 5b) have less commutations per cycle than the one generated by standard SPWM (Fig. 5a). Table III shows the combination of gate signals to achieve minimum switching frequency.

The value of the inverter capacitors is chosen to reduce switching ripple voltage beneath acceptable levels. The DC side inductors are selected in order to keep main current ripple below 1%. The current of the sharing inductors should have a ripple of less than 10%.

TABLE III
MINIMUM SWITCHING FREQUENCY GATE SIGNALS

Sequence	Module A Switch state							Output Current		
	State	A1	A2	A3	A4	A5	A6	IR	IS	IT
A	2	1				1		*I*/3	- *I*/3	0
	6			1		1		0	- *I*/3	*I*/3
	0		1			1		0	0	0
B	2	1				1		*I*/3	- *I*/3	0
	3	1					1	*I*/3	0	- *I*/3
	0	1			1			0	0	0
C	3	1					1	*I*/3	0	- *I*/3
	1		1				1	0	*I*/3	- *I*/3
	0			1			1	0	0	0
D	1		1				1	0	*I*/3	- *I*/3
	5		1		1			- *I*/3	*I*/3	0
	0		1			1		0	0	0
E	5		1		1			- *I*/3	*I*/3	0
	4			1	1			- *I*/3	0	*I*/3
	0	1			1			0	0	0
F	4			1	1			- *I*/3	0	*I*/3
	6			1		1		0	- *I*/3	*I*/3
	0			1			1	0	0	0

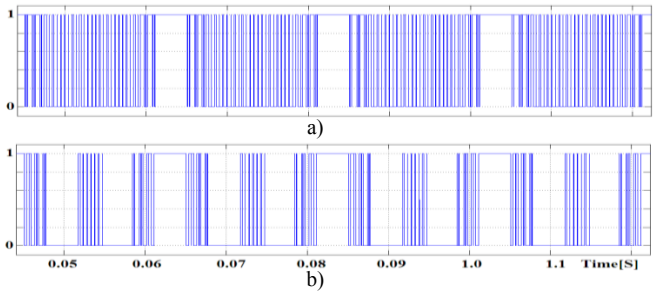

Fig. 5 – Gate signal for switch A1 a) SPWM b) sequential state machine.

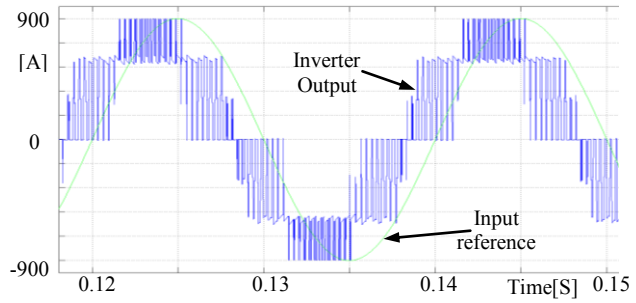

Fig. 6. Phase shift between input reference and inverter output currents

The modulation process generates a $\pi/6$ phase shift between the reference input and the current output of the inverter, as shown in Fig. 6. So, this should be taken into account by the control block, when generating the reference signals.

B. Control scheme and current reference generation

The control scheme of the inverter, shown in Fig. 7, is designed to compensate the reactive power and harmonic currents injected by the load. The control block measures the network phase voltages (Va, Vb, Vc) and load currents (i_{LFPa}, i_{LFPb}, i_{LFPc}), to build the reference currents for the MCSI. All the calculus is performed in a synchronous reference frame.

A three phase digital PLL generates the reference phase (θ) for the transformation to the rotating frame,

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \sin(\theta) & \sin(\theta - 2\pi/3) & \sin(\theta + 2\pi/3) \\ \cos(\theta) & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \end{bmatrix} \cdot \begin{bmatrix} i_{LFPa} \\ i_{LFPb} \\ i_{LFPc} \end{bmatrix} \quad (3)$$

After transformation of the measured load currents, the active (id) and reactive (iq) components are further divided in their mean values ($\bar{I}_d$, $\bar{I}_q$) and the alternate components ($\tilde{\imath}_d$, $\tilde{\imath}_q$). $\bar{I}_d$ is the current that should be supplied by the system, while the rest should be provided by the active filter. In order to lower the power rating of the inverter, the goal of the filter is to obtain a cos φ ≥ 0.96 instead of exactly 1.

The $\bar{I}_q$ is limited to the maximum design value, while $\tilde{\imath}_d$ and $\tilde{\imath}_q$ pass completely to built the reference currents to the inverter. The limit of $\bar{I}_q$ guarantees that the inverter functions without any saturation which may introduce undesired harmonics in the system. An additional control loop is added to control the active power the inverter can exchange with the system. This control loop allows the regulation of the DC current absorbing active power from the system. It is controlled by a PI controller that regulates the DC component

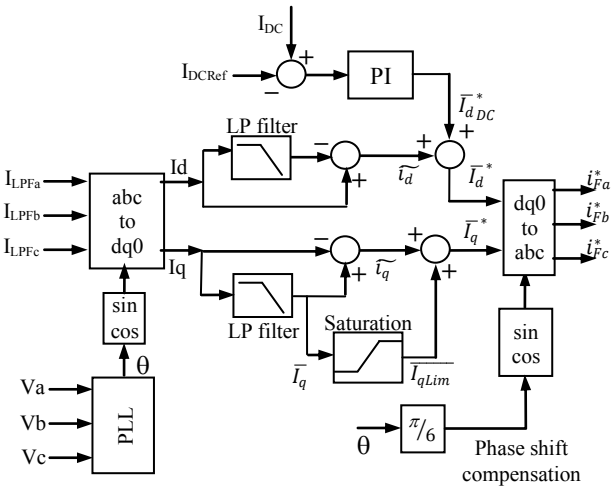

Fig. 7. Control Block

of $\bar{I}_d^*$. Active power can be exchanged between the inverter and the system, in both directions, to maintain Idc in a constant value.

$$I_d^* = \tilde{\imath}_d + \bar{I}_{d\,DC}^*$$
$$I_q^* = \tilde{\imath}_q + \bar{I}_{qLim} \quad (4)$$

Finally the dq0 reference signals (I_d^*, I_q^*) are transformed into abc reference signals (i_{Fa}^*, i_{Fb}^*, i_{Fc}^*). A π/6 phase shift is inserted in the dq0-to-abc transformation (4) to compensate the phase shift introduced by the modulation scheme.

$$\begin{bmatrix} i_{Fa}^* \\ i_{Fb}^* \\ i_{Fc}^* \end{bmatrix} = \begin{bmatrix} \sin\left(\theta - \frac{\pi}{6}\right) & \cos\left(\theta - \frac{\pi}{6}\right) \\ \sin\left(\theta - \frac{2\pi}{3} - \frac{\pi}{6}\right) & \cos\left(\theta - \frac{2\pi}{3} - \frac{\pi}{6}\right) \\ \sin\left(\theta + \frac{2\pi}{3} - \frac{\pi}{6}\right) & \cos\left(\theta + \frac{2\pi}{3} - \frac{\pi}{6}\right) \end{bmatrix} \begin{bmatrix} I_d^* \\ I_q^* \end{bmatrix} \quad (5)$$

IV. PERFORMANCE EVALUATION

The performance of the proposed system is simulated with Matlab Simulink Power System Blockset. The converter arrangement is composed by three identical modules to produce seven current levels. Each module is built with six IGBT's, with series diodes. The PSC-SPWM logic and the sequential state machine for each module are implemented with the StateFlow tool. The main parameters of the converter are summarized on Table IV.

The system's target is to obtain a displacement factor above 0.96 and to reduce the harmonic content below the limits fixed by IEEE, at full load.

At t = 50 ms the inverter is connected to the system, charging the main inductor for the next 50ms. The currents through the sharing inductors of the three modules are shown in Fig. 8. Balanced current sharing among all the modules of the MCSI inverter is maintained under all operating conditions. After the currents through the inductors arrive to their nominal value (t = 0.1 ms), the active filter improves the displacement factor and reduces the current harmonics.

TABLE IV
INVERTER PARAMETERS

Main current inductors	250 mH
Main DC current (nominal)	900 A
Sharing inductors	200 mH
System frequency	50 Hz
Coupling capacitors	5μF
Ripple filter	3μF 30Ω
Switching frequency	4065 Hz

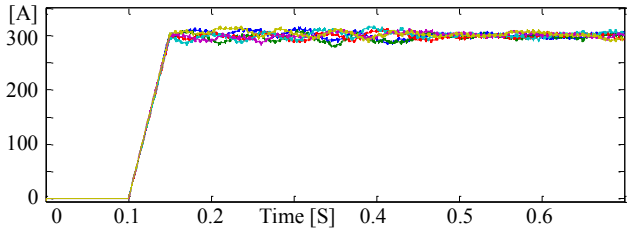

Fig. 8. Current through the sharing inductors of the MCSI

Fig. 9 shows how the system current in phase A becomes sinusoidal and almost in phase with system voltage. The spectra of the resulting system voltage and current are shown in Fig. 10 and 11. The voltage harmonic content in the system is reduced from 6.1% to 3.1% when the inverter compensates the 5th, 7th, 11th and 13th harmonics.

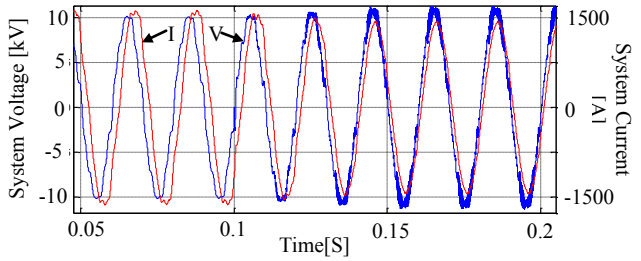

Fig. 9. Active filter startup: System voltage and current.

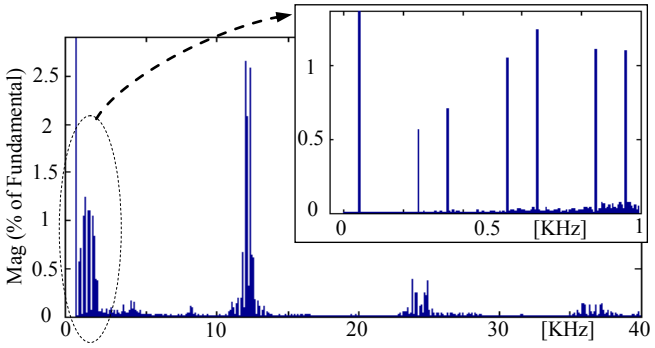

Fig. 10. System voltage spectra (Va) with compensation (and detail)
Fundamental 10.78 kV - THD=3.10%.

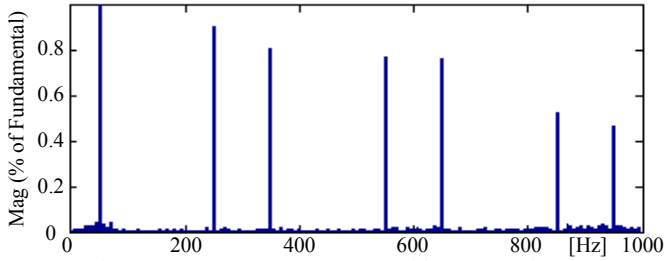

Fig. 11. System current spectra (Ia) with compensation.
Fundamental 1422 A - THD= 1.83%.

In order to consider the commutation frequency, both THD_V and THD_I have been calculated taking into account the harmonics up to 50KHz. The THD_V decreases to 1.90% when the harmonics are limited to the 50th order, as fixed by IEEE standards. No changes are seen in the THD_I. It can be seen that the effective switching frequency of the inverter is three times the frequency of each module due to the multilevel and phase shift carrier modulation.

Transient behavior is evaluated with a load reduction of 25% at t=0.4s. Such reduction is shown in Fig. 12. Table V summarizes the system performance under both load conditions. Since the inverter is designed to compensate the maximum available reactive power, the resulting power factor at 75% load is 0.99.

Fig. 13 shows the powers supplied by the system during start up, full load and after load reduction. At full load, the inverter provides the load with an average value of Q_{INV} = 11.8 MVAr. The load needs Q_{LOAD} = 17.8 MVAr, so the system only provides Q_{SYSTEM} = 6 MVAr. The active power supplied by the system at full load is 22.2MW with cosφ = 0.965.

Since the load is modeled as constant shunt impedance, its needs of active and reactive power varies with the square of the voltage applied to it. The voltage across the load increases when the active filter compensates reactive power, causing an increment of active and reactive power in the load. The compensation of 11.8 MVAr, at full load, produces an increment of 5.7% in the voltage at 13.8 kV bus bar and a consequent increment of 1.9 MVAr in the reactive power taken by the load, as shown in Fig. 13.

The current waveform generated by the inverter before the ripple filter is shown in Fig. 14a, where the seven levels predicted by (1) are clearly seen. The current the active filter injects into the system (I_{Fa}) is shown in Fig. 14b.

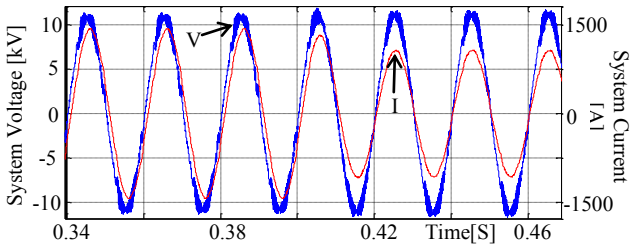

Fig. 12. Load decrease by 25%. System voltage and current

TABLE V
HARMONIC VOLTAGES RESULTS AND VERIFICATIONS WITH COMPENSATION

Harmonic Voltages	100 % load	75 % load	IEEE Limits
V_5 (%)	0.56	0.49	3
V_7 (%)	0.70	0.64	3
V_{11} (%)	1.05	0.93	3
V_{13} (%)	1.24	1.03	3
THD_V (%)	3.10	2.43	5

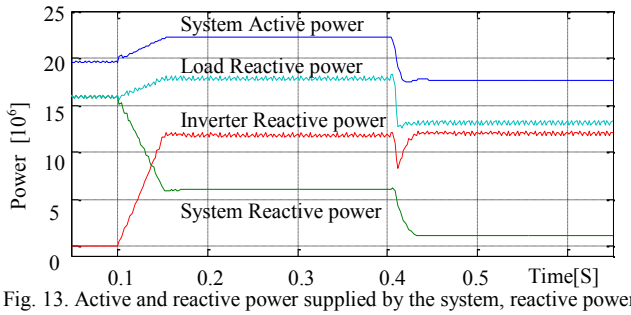

Fig. 13. Active and reactive power supplied by the system, reactive power provided by the inverter

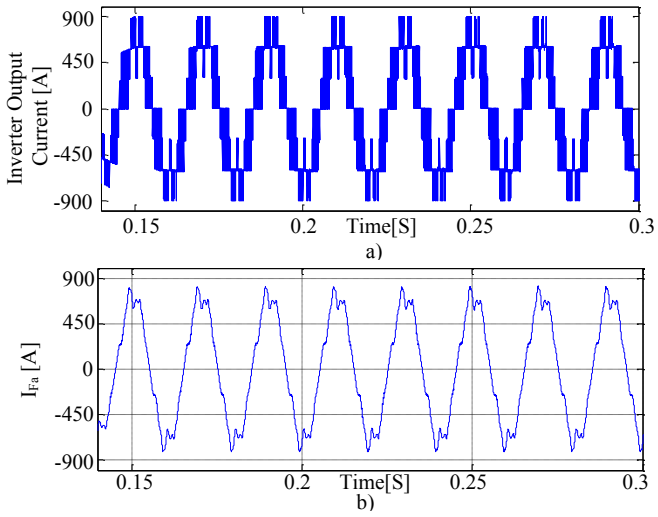

Fig 14. Active filter current: a) current produced by the inverter, b) current injected into the system.

V. CONCLUSIONS

A novel modular single rating inductor MCSI topology was proposed in this paper to compensate Power Quality problems in a distribution network. As a result of circuit topology and PSC-SPWM utilization, current balance was achieved in both main and sharing inductors, in steady state and transient conditions. The switching frequency was minimized with a state-machine approach, taking the advantage of the three different zero-states of the topology.

The design of a shunt active filter, built with a MCSI, to compensate reactive power and harmonics in the medium voltage level of a power distribution system was presented in this paper. The proposal shows very good performance and it is an interesting alternative to VSI implementation of active filters.

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