

# Measurements and Studies of Harmonics and Switching Transients in Large HV Shunt Capacitor Banks

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**Abstract**—Adding capacitors to an electric power system provides well known benefits, including power factor correction, voltage support and increase of active power transfer capacity. However, the capacitor banks modify the harmonic voltages and currents in the network and give rise to current and voltage transients, stressing switching devices and sensitive loads.

The first part of the paper describes measurements and studies performed before the installation of 2x50 MVar capacitor banks in a 500-132 kV substation, in the Argentinian Transmission System. By measurements of harmonics content in voltage and current, the IITREE performed some studies to quantify the harmonic voltage in the 132 kV busbar and the harmonic voltages and currents in the capacitors to prevent excessive overload. Switching Transients were also studied. The studies carried out with the Electromagnetic Transients Program (EMTP) are presented.

The second part of the paper deals with measurements performed after the installation of the 2x50 MVar capacitor banks. These measurements were carried out to verify the harmonic levels in the busbar and in the capacitor bank, and to obtain the current and voltage switching transients. The results of measurements are compared to the ones obtained by studies and simulations.

**Index Terms**—Harmonics, THD, switching transients, inrush current, overvoltage, restrike, surge arresters.

## I. INTRODUCTION

Shunt capacitors supply reactive power and boost local voltages. They are used throughout the system and are applied in a wide range of sizes. The principal advantages of shunt capacitors are their low cost and their flexibility of installation and operation. The main disadvantage of shunt capacitors is that their reactive power output is proportional to the square of the voltage. Consequently, the reactive power output is reduced at low voltages when it is most needed [1].

Shunt capacitors are used extensively in distribution systems for power-factor correction and feeder voltage control [2]. Shunt capacitors are also used to compensate the  $XI^2$  losses in transmission systems and to ensure satisfactory voltage levels during heavy loading conditions. Capacitor banks are connected either directly to the high voltage bus or to the tertiary winding of the main transformer.

Switching off capacitor banks provides a convenient means of controlling transmission system voltages. They are normally distributed throughout the transmission system so as to minimize losses and voltage drops. Detailed power-flow studies are performed to determine the size and location of capacitor banks to meet the system design criteria.

This paper presents measurements and studies performed before the installation of 2x50 MVar capacitor banks in a 500-132 kV substation, in the Argentinian Transmission System. The studies performed predicted the harmonics levels in the 132 kV busbar and in the capacitors. Switching transients, including energizing and de-energizing phenomena were also studied.

After the installation of the capacitor banks, the IITREE performed new measurements to verify the harmonics on the capacitors and in the 132 kV busbar, and to verify the capacitor bank energizing and de-energizing transients.

The evaluation of the power quality of contemporary International and Argentinian standards is given, and the fundamental parameters of harmonic levels and switching transients are compared to reference values established by International Standards.

## II. POWER SYSTEM CONFIGURATION

The power system one-line diagram is shown in Fig. 1.

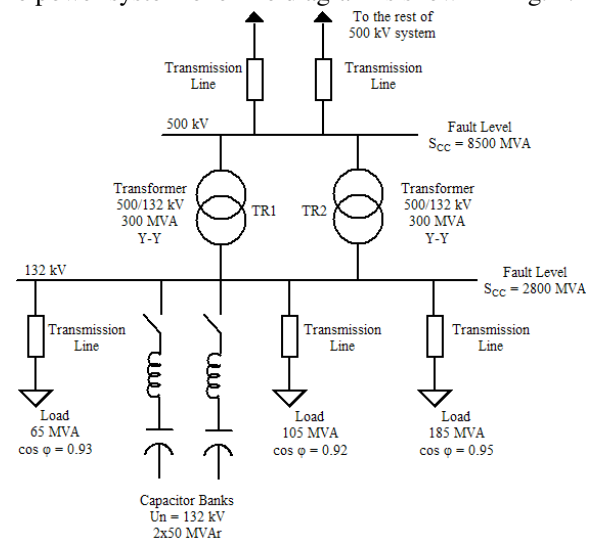


Fig. 1: One-line diagram of the power system.

The substation is composed by two 500/132 kV, 300 MVA transformers. The capacitor bank contains two 50 MVar fixed steps, for a total of 100 MVar at 132 kV. The technical installation specifications are shown in Table I to Table III.

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Table I: Capacitor Bank technical specifications.

Capacitor Bank	Single Unit	Complete Bank
Manufacturer	Leyden SA	
Reactive Power	417 KVAR	50 MVAR
Nominal Voltage	7.62 kV	132 kV
Nominal Capacitance	22.86 $\mu$ F	9.13 $\mu$ F
Nominal Current	54.7 A	218.7 A

**Shunt capacitor bank arrangement:**

Each phase: H-bridge connection

Between phases: ungrounded single wye

Series per phase: 10

Parallels per phase: 4

Total of capacitors of each bank: 120

There are current transformers (CT) connected between legs. In the case of an internal failure of a capacitor the internal fuse will operate (isolating only the element which has failed) and a small current will flow between legs. The unbalance CT is capable of sensing the unbalance current between both legs of a phase (in the crossbar of the H-bridge).

Table II: Reactor technical specifications.

Reactor	
Manufacturer	Trench
Nominal Inductance	900 $\mu$ H
Nominal Impedance	0.28 $\Omega$
Nominal Current	315 A
Nominal Voltage	132 kV
Reactive Power	27.78 kVAR

Table III: Surge Arrester technical specifications.

Surge Arresters	EXLIM P
Manufacturer	ABB
Rated Voltage ( $U_r$ )	120 kV
Continuous operating voltage (IEC) $U_c$	78 kV
Continuous operating voltage (ANSI) MCOV	98 kV
Nominal Discharge current (IEC)	20 kA
Energy capability (single impulse of 4 ms duration)	$\frac{7kJ}{kV} U_r$

**III. HARMONIC MEASUREMENTS**

Before the installation of the capacitor banks, the voltage harmonic levels in the 132 kV busbar and the current harmonics in the secondary windings of the two power transformers were measured. The results obtained for a normalized one-week measurement of voltage levels are shown in Fig 2, and summarized in Table IV.

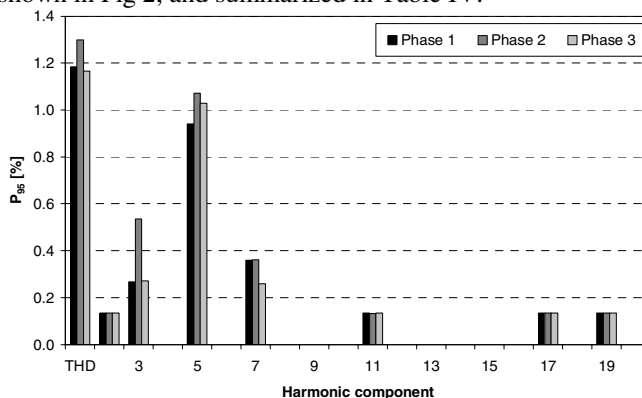


Fig. 2: Voltage harmonic measurements.

The Argentinian Standard for voltage harmonic distortion is ENRE's Res. 184/00 [5]. This Standard is based on IEC 61000-3-6 Standard and defines the voltage harmonic limits according to the voltage level.

The IEEE 519-1992 [6] is an American Standard which also defines voltage harmonic limits according to the voltage level. Both limits are included as reference values in Table IV.

Table IV: Reference levels for voltage harmonics according to ENRE and IEEE and measured voltage harmonics.

	THD	H3	H5	H7	H11	H17	H19
<b>ENRE Limits</b>	3	1.5	2	1.5	1.5	1	1
<b>IEEE Limits</b>	2.5	1.5	1.5	1.5	1.5	1.5	1.5
<b>Medium</b>	0.82	0.14	0.60	0.07	0.06	0.12	0.13
<b>P95</b>	1.22	0.36	1.01	0.33	0.13	0.13	0.13
<b>Maximum</b>	1.54	0.40	1.35	0.39	0.17	0.13	0.18

The results obtained for one-week measurements of current levels in the secondary of both transformers are shown in Fig 3 and Fig 4, and summarized in Tables V and Table VI.

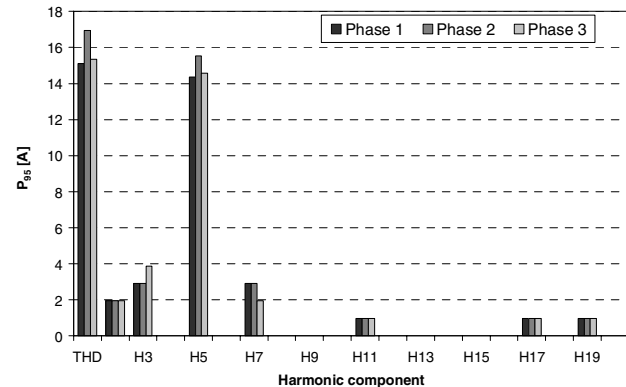


Fig. 3: Current harmonic measurements in TR1.

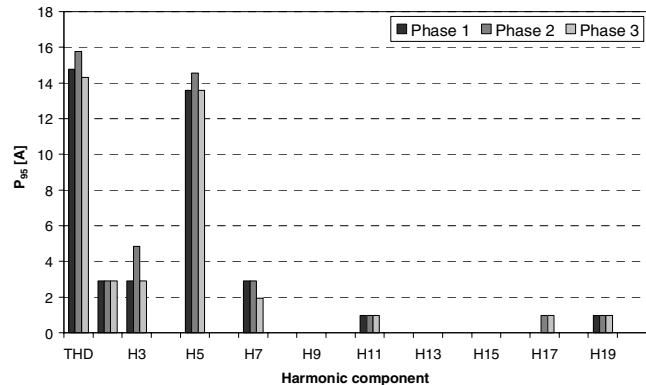


Fig. 4: Current harmonic measurements in TR2.

Table V: Current harmonics measured in TR1 [A].

	TDD	H3	H5	H7	H11	H17	H19
<b>Medium</b>	11.81	1.51	10.74	1.38	0.13	0.21	0.80
<b>P95</b>	15.79	3.24	14.83	2.59	0.77	0.77	0.87
<b>Maximum</b>	17.50	3.88	16.51	3.56	0.97	0.97	0.97

Table VI: Current harmonics measured in TR2 [A].

	TDD	H3	H5	H7	H11	H17	H19
<b>Medium</b>	10.82	2.01	9.50	1.00	0.16	0.07	0.72
<b>P95</b>	14.96	3.56	13.92	2.59	0.67	0.75	0.84
<b>Maximum</b>	16.96	3.88	16.19	2.91	0.97	0.97	0.97

## IV. HARMONIC AND SWITCHING TRANSIENT STUDIES

### A. Harmonic calculations and studies

Adding capacitors will cause the power system to be tuned to a specific harmonic. This is known as parallel resonance between the capacitors and the source inductance (including the transformer). A parallel resonance presents a high impedance to injected harmonics near the resonant frequency. The resonant frequency of a capacitor can be estimated by:

$$h = \sqrt{\frac{S_{CC}}{Q}} \quad (1)$$

Where:

$S_{CC}$  is the short-circuit power (MVA) at the point where the capacitor is to be connected.

$Q$  is the rated reactive power (MVar) of the capacitor.

$h$  is the harmonic number.

The results for both alternatives are shown in Table VII.

Table VII: Harmonic resonance.

Bank Q [MVar]	$S_{CC}$ [MVA]	$h$	$f$ [Hz]
50	2800	7.48	374.2
100	2800	5.29	264.6

Frequency scan analysis is used to characterize the response of a power system as a function of frequency. This analysis is based on a frequency-variable current source. The value of the obtained voltage is proportional to the desired impedance.

Frequency scan studies begin with a detailed system model, including transmission lines, transformers and loads. Key modeling features for this case were:

- Transmission lines were modeled using a distributed-parameter line model.
- Generators were modeled as a shunt equivalent reactance. This reactance is the sub-transient one.
- Transformers were modeled as a resistance in series with the leakage inductance.
- Loads were modeled as constant parallel R-L impedances.

The results obtained for the impedance at 132 kV busbar, for three different system configurations are shown in Fig 5.

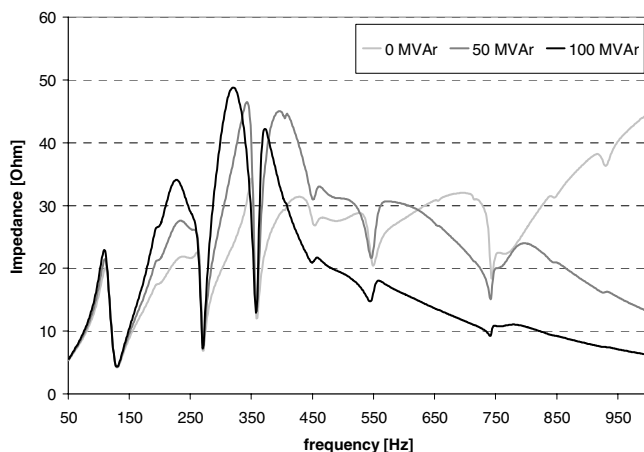


Fig. 5: Plot of Impedance magnitude in the 132 kV busbar.

The impedance values at the three different operating conditions are shown in Table VIII.

Table VIII: Impedance in the 132 kV busbar.

Capacitor bank condition	Z1 (Ω)	Z3 (Ω)	Z5 (Ω)	Z7 (Ω)	Z11 (Ω)	Z17 (Ω)	Z19 (Ω)
0 MVar	5.39	8.99	21.64	34.29	20.54	31.65	40.25
50 MVar	5.47	9.72	26.28	38.96	23.55	20.92	15.41
100 MVar	5.56	10.57	28.99	26.91	16.47	9.25	7.13

The impedance increment or decrement is proportional to the 132 kV voltage distortion increment or decrement. From Table VII it is possible to distinguish a 33% increment in the 5<sup>th</sup> harmonic impedance, in the case of two banks connected.

To evaluate the modification of voltage distortion in the 132 kV busbar with the presence of the capacitor bank, some current sources representing the 3<sup>rd</sup>, 5<sup>th</sup> and 7<sup>th</sup> harmonics were introduced in the model. The amplitude of the current sources was adjusted so as to reproduce the measured voltage harmonic distortion in the 132 kV busbar and current harmonic distortion in the secondary side of power transformers.

The results obtained for the 500 kV and 132 kV busbars, with different combinations of shunt capacitors are shown in Fig. 6 and Fig. 7. The results are also summarized in Table IX and Table X.

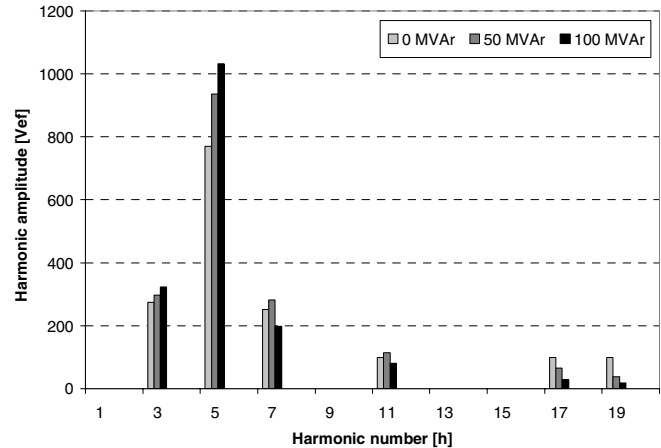


Fig. 6: Voltage harmonic distortion in 132 kV busbar.

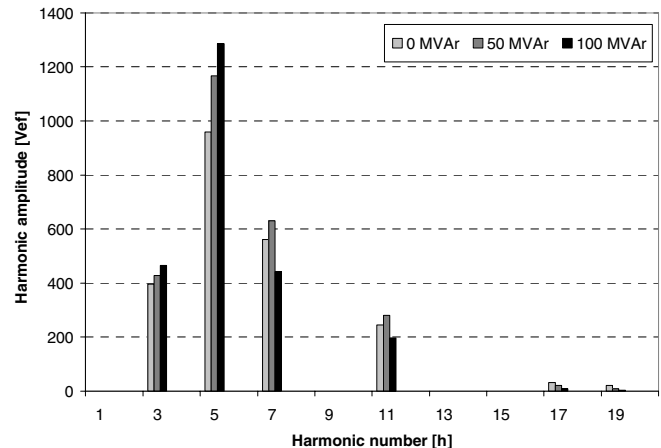


Fig. 7: Voltage harmonic distortion in 500 kV busbar.

In Table IX and Table X the voltage harmonic distortion in 132 kV and 500 kV are expressed in percent of the corresponding rated value. Additionally, the reference level according to IEEE 519-1992 and ENRE 184/00 are presented.

Table IX: Voltage harmonic distortion in 132 kV.

	THD	H3	H5	H7	H11	H17	H19
<b>ENRE Limits</b>	3	1.5	2	1.5	1.5	1	1
<b>IEEE Limits</b>	2.5	1.5	1.5	1.5	1.5	1.5	1.5
<b>0 MVar</b>	1.20	0.36	1.01	0.33	0.13	0.13	0.13
<b>50 MVar</b>	1.41	0.39	1.23	0.37	0.15	0.09	0.05
<b>100 MVar</b>	1.51	0.61	<b>1.69</b>	0.58	0.26	0.01	0.01

Table X: Voltage harmonic distortion in 500 kV.

	THD	H3	H5	H7	H11	H17	H19
<b>ENRE Limits</b>	1.5	0.75	1	1	0.75	0.5	0.5
<b>IEEE Limits</b>	1.5	1	1	1	1	1	1
<b>0 MVar</b>	0.42	0.14	0.33	0.19	0.08	0.01	0.01
<b>50 MVar</b>	0.49	0.15	0.40	0.22	0.10	0.01	0.01
<b>100MVar</b>	0.42	0.16	0.45	0.15	0.07	0.01	0.01

The voltage harmonic distortion in 132 kV and 500 kV was below the limits established by ENRE, but for the particular case of 5<sup>th</sup> harmonic, it exceeded the IEEE limit in 132 kV.

Capacitors must be built to tolerate voltages and currents in excess to their ratings according to standards. The applicable standards for shunt power capacitors are IEEE Standard 18-1992 [7] and IEC 60871-1 [8].

IEEE Standard 18-1992 yields the following allowable contingency overload limits:

- 110% of rated rms voltage
- 120% of rated peak voltage
- 180% of rated rms current (nominal current based on rated reactive power and voltage)

IEC Standard 60871-1 yields the following allowable contingency overload limits:

- 110% of rated rms voltage (12 hours every 24 hours)
- 130% of rated current (nominal current based on rated reactive power and voltage)

The IEC 60871-1 overload current limits are more restrictive than IEEE 18-1992.

The results obtained by EMTF simulations for the voltage and current harmonic distortion in the capacitors are shown in Table XI and Table XII.

The adopted value for the fundamental component of capacitor voltage is  $1.08 \times U_{N\text{system}}$ . This 1.08 factor results from the addition of the maximum operating voltage of 132 kV busbar ( $1.05 \times U_{N\text{system}}$ ) and from the permanent increase of system voltage because of the capacitor. This increment in the system voltage at the point of connection of capacitor banks can be estimated by:

$$\frac{\Delta U}{U} \approx \frac{Q}{S_{CC}} \cdot 100 = \frac{100 \times 10^6}{2800 \times 10^6} \cdot 100 = 3.6\% \quad (2)$$

Table XI: Voltage harmonic distortion in the capacitor bank.

	H1 [V]	H3 [V]	H5 [V]	H7 [V]	H11 [V]	$U_{rms}/U_N$ [%]	IEC [%]
<b>50 MVar</b>	82307	299	955	293	126	108	110
<b>100 MVar</b>	82307	326	1053	205	88	108	110

Table XII: Current harmonic distortion in the capacitor bank.

	H1 [A]	H3 [A]	H5 [A]	H7 [A]	H11 [A]	$U_{rms}/U_N$ [%]	IEC [%]
<b>50 MVar</b>	236.1	2.6	13.7	5.9	4.0	108	130
<b>100 MVar</b>	236.1	2.8	15.1	4.1	2.8	108	130

For both operating conditions of capacitor banks, none of the values established were exceeded in the simulations.

### B. Capacitor switching transients

On connecting a capacitor to a power source, the voltage of the bus to which the capacitor is connected will be pulled down to zero momentarily. The voltage on the capacitor will present a high-frequency oscillation around the 50 Hz fundamental waveform. This oscillation will gradually get damped in few cycles. The damping is a function of the resistance and losses in the system.

The magnitude of the transient will vary based on two variables at the moment of switching: The initial voltage on the capacitor and the instantaneous system voltage at the time of switching. The greater the difference between these two voltages, the greater the magnitude of the current transient.

Back-to-back switching involves energizing a capacitor bank on the same bus when another energized bank is already energized. In this case, a fast transient occurs as the two capacitors share their charge and come to the same voltage. In this case, the current magnitude will be limited by the inductance between the banks, defined by the sum of the series reactors. This inductance is comparatively much smaller than the source inductance, so the magnitude and the frequency of the inrush current will be higher.

The frequency and magnitude limits of the inrush current during the switching of a capacitor bank are described in the IEC-62271-100 Standard [9]. This Standard is focused on high voltage alternating current circuit breakers and defines the rated capacitive switching currents. The preferred values mentioned in that standard are reproduced in Table XIII.

Table XIII: Preferred values of rated capacitive currents.

Single capacitor bank or Back-to-back capacitor bank			
Breaking current [A]	Crest current [kA]	frequency [Hz]	product I <sub>s</sub> f [AxHz]
400	20	4250	85x10 <sup>6</sup>

The values mentioned in the Standard are independent from the rated voltage of the capacitor bank.

IEC 60871-1 Standard establishes that the peak value of the overcurrents due to switching operations should be limited to a maximum of  $I_s = 100 \times I_N$  (rms value of nominal current). The transient overvoltage caused by the energization of a

capacitor bank should not exceed  $2\sqrt{2}$  times the applied voltage (rms value) for a maximum duration of 1/2 cycle.

The IEC 60871-1 and IEC 62271-100 Standards suggest some formulae for calculating the inrush current of a capacitor bank. Those formulae are reproduced in Table XIV.

Table XIV: Capacitor inrush current calculation according to International Standards.

Standard	60871-1	62271-100
Single Bank	$\hat{I}_s = I_N \sqrt{\frac{2S_{CC}}{Q}}$	$\hat{I}_s = U \sqrt{\frac{2C}{3(L_0 + L)}}$ $f = \frac{1}{2\pi\sqrt{C \cdot (L_0 + L)}}$
Back to Back	$\hat{I}_s = \frac{U\sqrt{2}}{\sqrt{X_C X_L}}$ $X_C = 3U^2 \left( \frac{1}{Q_1} + \frac{1}{Q_2} \right)$	$\hat{I}_s = U \sqrt{\frac{2}{3} \frac{C_1 C}{(C_1 + C)(L_1 + L)}}$ $f = \frac{1}{2\pi\sqrt{\frac{C_1 C}{(C_1 + C)(L_1 + L)}}$

Where:

$\hat{I}_s$  is the crest of inrush bank current in [A].

$I_N$  is the rated bank current in [A].

$U$  is the phase-to-ground voltage in [V].

$X_C$  is the series-connected capacitive reactance per phase between the banks in [ $\Omega$ ].

$X_L$  is the inductive reactance between banks in [ $\Omega$ ].

$Q_1$  is the output of the bank to be switched on, in [MVar]

$Q_2$  is the sum of the output of the already energized bank(s) in [MVar].

$f$  is the inrush current frequency in [Hz].

$L_0$  is the source inductance in [H].

$L$  is the inductance in series with switched bank in [H].

$C$  is the capacitance of the switched bank in [F].

$C_1$  is the capacitance of the previously connected bank.

The results obtained in the EMTF simulations for the energization of the single capacitor bank are shown in Fig. 8 and Fig. 9. Table XV summarizes the results obtained by calculations and by EMTF simulations for the inrush transient current.

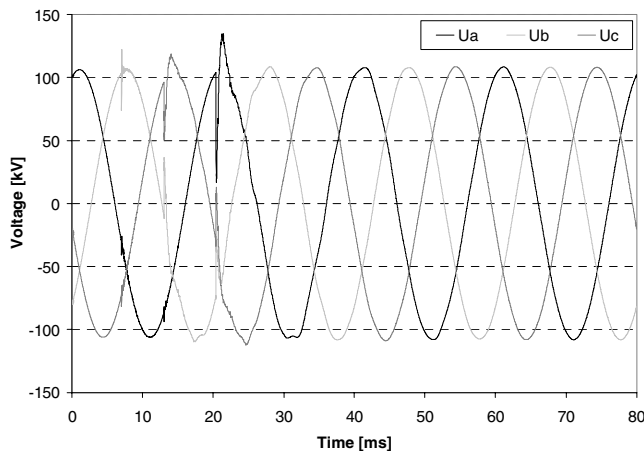


Fig. 8: Simulated capacitor phase-to-ground voltages.

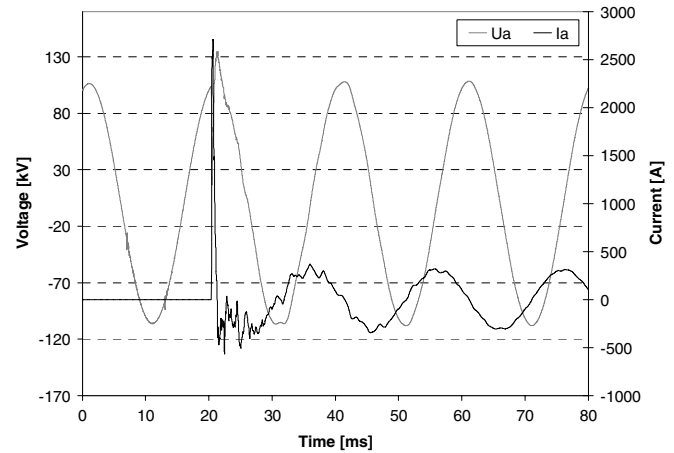


Fig. 9: Simulated capacitor voltage and current.

Table XV: Results for connection of a single bank.

$U_{amax}$ [kV]	$U_{acmax}$ [kV]	$I_{smax}$ [A] (calculated)	$I_{smax}$ [A] (simulated)	frequency [Hz] (calculated)
135	213	2315	2707	366

The results obtained in the EMTF simulations for the back-to-back energization are shown in Fig. 10 and Fig. 11.

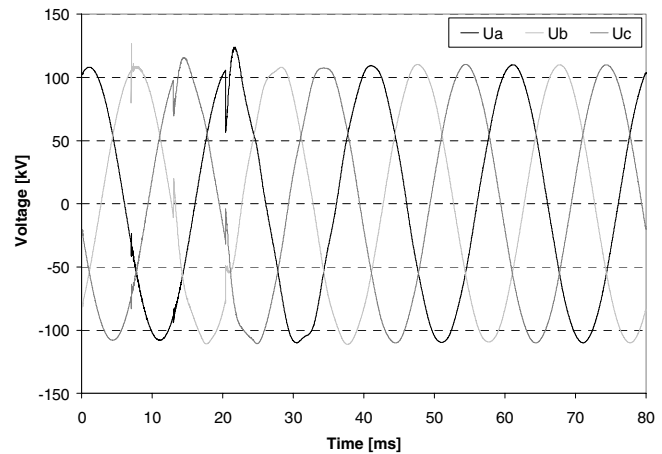


Fig. 10: Simulated capacitor phase-to-ground voltages.

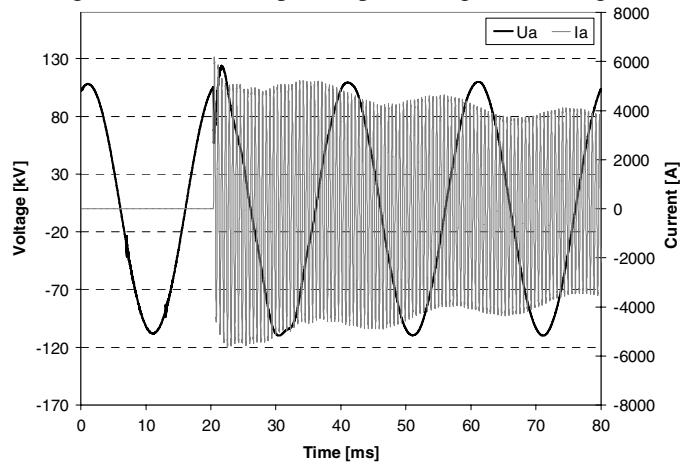


Fig. 11: Simulated capacitor voltage and current.

Table XVI summarizes the results obtained by calculations and by EMTF simulations for the Back-to-back inrush transient current.

Table XVI: Results for connection of a single bank.

$U_{amax}$ [kV]	$I_{smax}$ [A] (calculated)	$I_{smax}$ [A] (simulated)	frequency [Hz] (calculated)	frequency [Hz] (simulated)
124	5429	6177	1755	1740

The difference in the calculated and simulated inrush current peak value in both cases (single bank connection and back-to-back connection) is due to the effect of the shunt capacitances of the high voltage transmission lines.

The circuit breaker interrupts current around a current zero and the capacitor is charged to full voltage after current interruption. The voltage at the supply side oscillates at a frequency given by the supply side inductance and the capacitance, and the difference between these two voltages appears across the breaker pole. This voltage can be more than twice the rated voltage.

If the gap across the breaker has not recovered enough dielectric strength, it breaks down and produces an electric arc between contacts. The capacitor which is being disconnected is reconnected to the power system. This result in a high frequency overvoltage superimposed to 50 Hz system voltage.

Phase-to-ground surge arresters were installed to limit these overvoltages. To evaluate the protective action of the installed surge arrester, a de-energizing action followed by a current restrike was simulated in EMTP. The results obtained from simulations are shown in Fig. 12 and Fig. 13.

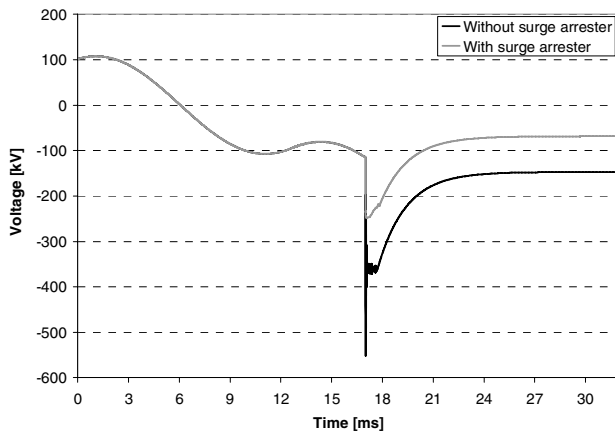


Fig. 12: Phase-to-ground voltage 1 in the Capacitor bank, with and without surge arrester.

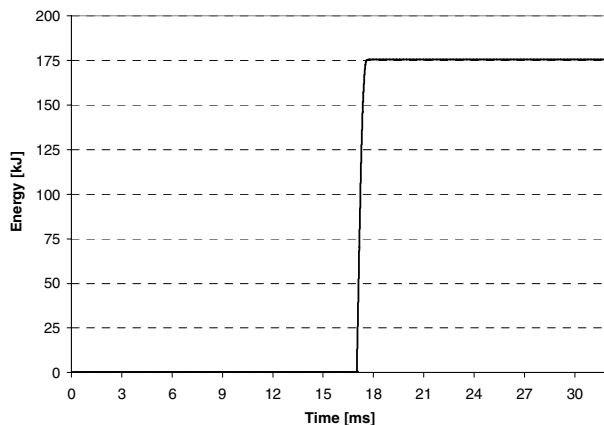


Fig. 13: Energy dissipation through phase-to-ground arrester.

The capacitor overvoltage during a current restrike can reach values as high as 550 kV. With a phase-to-ground surge arrester this overvoltage is reduced to 250 kV.

The energy dissipation in the surge arrester is 175 kJ. This value is below the energy capability of the installed surge arrester, which is equal to 840 kJ.

## V. HARMONIC AND SWITCHING MEASUREMENTS

After the installation of the capacitor banks, and during the commissioning program, the IITREE performed new measurements to verify the harmonics in the capacitor banks and in the 132 kV busbar. The capacitor banks energizing and de-energizing transients were also recorded.

Some petrochemical plants are fed from this substation. Those plants could suffer the effect of energizing and de-energizing transients on some susceptible equipment, so the first measurements were carried out by using two isolated busbar. One busbar feeding the industrial load and the other one feeding the capacitor banks. This is an abnormal situation, (the two 132 kV busbars always operate as only one busbar) which was not previously studied.

Voltage and current harmonic distortion in the capacitor bank are shown in Fig. 14 and Fig. 15.

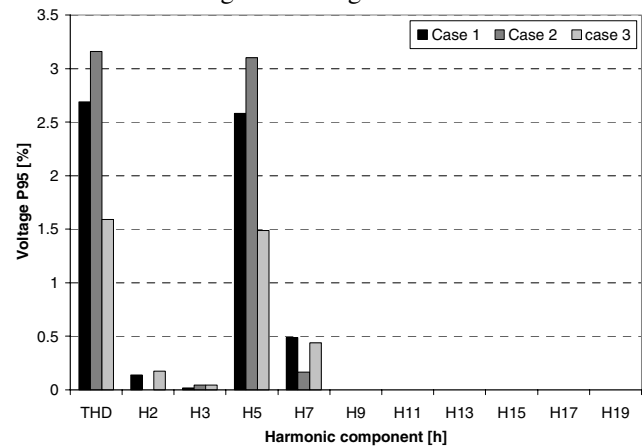


Fig. 14: Voltage harmonic distortion in 132 kV busbar.

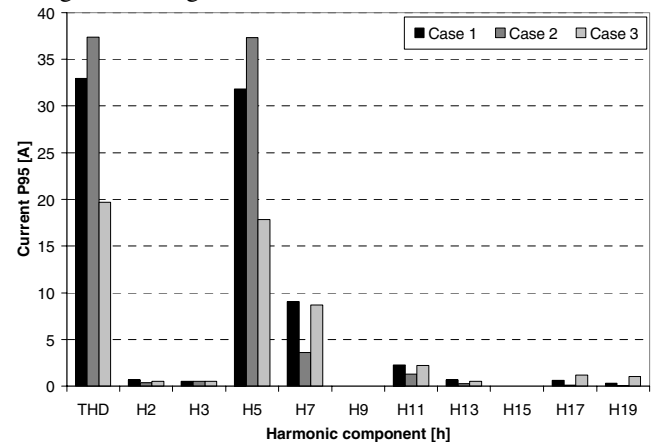


Fig. 15: Current harmonic distortion in the capacitor banks.

The performed measurements were:

*Case 1:* One capacitor bank connected to one 132 kV busbar, with the petrochemical load isolated from that busbar.

**Case 2:** Two capacitor banks connected to one 132 kV busbar, with the petrochemical load isolated from that busbar.

**Case 3:** Two capacitor banks connected to one 132 kV busbar, with the entire load connected to that busbar.

The Case 3 is the normal operating condition, and was analyzed in detail in the studies. Table XVII and Table XVIII summarize the voltage and current harmonic distortion in the capacitor in the different operating conditions.

Table XVII: Voltage harmonic distortion in 132 kV.

	THD	H3	H5	H7	H11	H17	H19
<b>ENRE Limits</b>	3	1.5	2	1.5	1.5	1	1
<b>IEEE Limits</b>	2.5	1.5	1.5	1.5	1.5	1.5	1.5
<b>Case 1</b>	<b>2.53</b>	0.06	<b>2.43</b>	0.27	0	0	0
<b>Case 2</b>	<b>3.13</b>	0.13	<b>3.05</b>	0.13	0	0	0
<b>Case 3</b>	1.71	0.13	1.58	0.53	0	0	0

Table XVIII: Current distortion in the capacitor bank.

Bank	H1 [A]	H3 [A]	H5 [A]	H7 [A]	H11 [A]	$U_{rms}/U_N$ [%]	IEC [%]
<b>Case 1</b>	236	0.3	30.4	6.4	1.7	109	130
<b>Case 2</b>	232	0.3	37.1	3.3	1	108	130
<b>Case 3</b>	240	0.5	18.9	8	1.7	110	130

The results obtained for voltage and current harmonic distortion in case 3 are similar to the ones predicted by the harmonic studies.

#### Switching Transients: single capacitor bank energization.

The results obtained from measurements of voltage and current in the single bank energization are shown in Fig. 16 and Fig. 17.

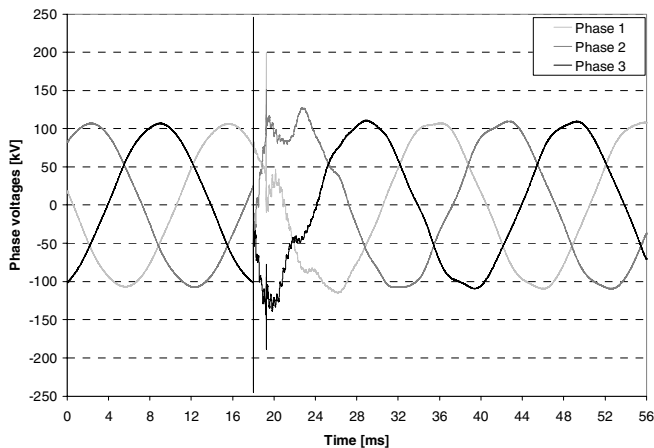


Fig. 16: Measured capacitor phase-to-ground voltages.

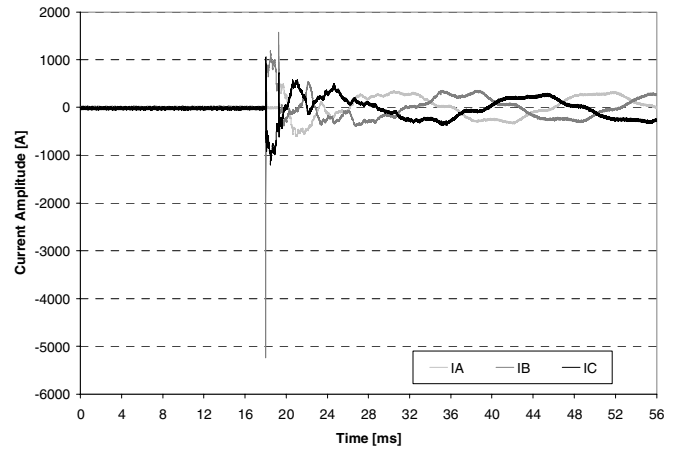


Fig. 17: Measured capacitor currents.

#### Switching Transients: Back-to-back energization.

The measurements of voltage and current in the back-to-back capacitor energization are shown in Fig. 18 and Fig. 19.

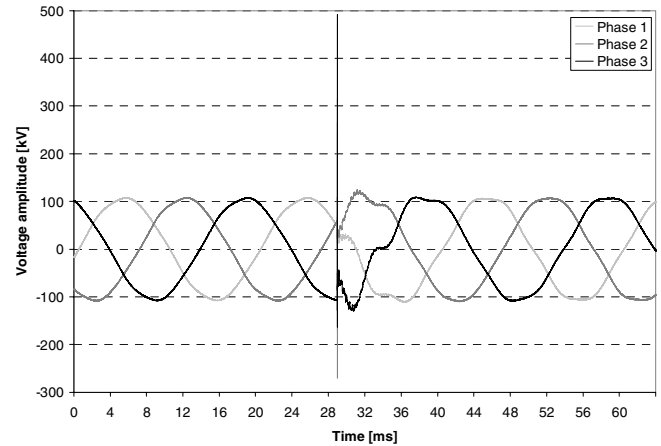


Fig. 18: Measured capacitor phase-to-ground voltages.

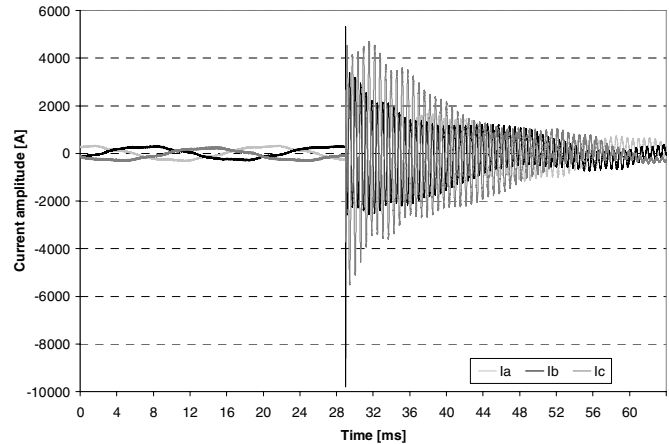


Fig. 19: Measured capacitor currents.

The results obtained from the measurement are presented in Table XIX for the single bank energization and in Table XX for the Back-to-back energization. The values estimated by studies and calculations are also included.

Table XIX: Results for single bank energization.

$U_{\text{phase}}$ [kV] measured	$U_{\text{phase}}$ [kV] simulated	$I_{\text{smax}}$ [A] measured	$I_{\text{smax}}$ [A] simulated	$I_{\text{smax}}$ [A] calculated
200	135	1940	2707	2315

Table XX: Results for Back-to-back energization.

$U_{\text{phase}}$ [kV] measured	$U_{\text{phase}}$ [kV] simulated	$I_{\text{smax}}$ [A] measured	$I_{\text{smax}}$ [A] simulated	$I_{\text{smax}}$ [A] calculated
130	124	5984	6177	5429

All the measured transient overvoltages were below the substation BIL (Base Insulation Level) of 550 kV.

The first current peak observed in measurements resulted from the charge transfer between the stray capacitance to ground of 132 kV busbar and the stray capacitance to ground of the overall bank and its housing. This first peak was recorded because that current circulated in the CT but not through the capacitors and was not considered in the evaluation. The peak value was also measured in the 132 kV busbar voltage. This high-frequency transient (shorter than 10  $\mu\text{s}$ ) was over the CT and PT measuring bandwidths, so it was only considered as an indicative value.

#### Switching Transients: single capacitor de-energization.

The measurements of voltage and current in the single capacitor de-energization are shown in Fig. 20.

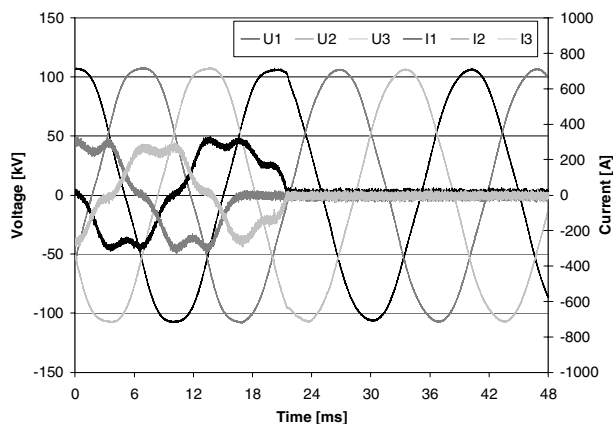


Fig. 20: Measured capacitor currents.

According to measurements, there were no current restrikes during the disconnection of the capacitor bank.

## VI. CONCLUSIONS

In this paper, is it described the complete technical procedure to study the effect of large shunt capacitor banks. The measurements performed prior to the installation of banks are used in a detailed EMTF model of the network to predict the harmonic distortion in the busbar and in the banks when they are connected. The results obtained for voltage and current harmonic distortion present a good agreement with measurements performed in the capacitor banks.

An important conclusion about the harmonic studies with capacitor banks is that the rated voltage of the bank should be equal to the maximum operating voltage of the busbar.

The maximum operating voltage can be 10 % higher than the rated network voltage.

There were slight differences between the simulated and measured magnitude of the inrush current. This is due to stray capacitances and inductances present in the real circuit.

It is the aim of this paper to prove the importance of performing previous and subsequent measurements in relation to electromagnetic studies when large shunt capacitor banks are installed in power systems.

## VII. REFERENCES

- [1] Allan Greenwood, *Electrical Transients in Power Systems*, 2nd Ed. New York: Wiley, 1991. ISBN: 0471620580.
- [2] Prabha Kundur, *Power Systems Stability and Control*, McGraw-Hill Professional, 1994. ISBN: 007035958X.
- [3] "Analysis and control of Large-Shunt-Capacitor-Bank Switching Transients". J. C. Das. Pp. 1444-1451. 0093-9994/2005.
- [4] "Capacitor Failure Analysis". T. M. Blooming. Pp 38-48. IEEE IAS Magazine. ISSN: 1077-2618/06.
- [5] *Base Metodológica para el Control de la Calidad del Producto Técnico*. Etapa 2. Ente Nacional Regulador de la Electricidad. Resolución ENRE 184/00, 2000.
- [6] *IEEE Recommended Practices and Requirements for Harmonics Control in Electrical power Systems*. IEEE Std. 519-1992.
- [7] *IEEE Standard for Shunt Power Capacitors*, IEEE Standard 18-1992.
- [8] *Shunt capacitors for a.c. power systems having a rated voltage above 1000 V*. Part 1. General. IEC Standard 60871-1, 1997.
- [9] *High Voltage Switchgear and Controlgear*. Part 100. High-voltage alternating-current circuit breakers. IEC Standard 62271-100, 2001.

## VIII. BIOGRAPHIES



**Pedro Eduardo Issouribehere** received the Engineer degree from La Plata National University, Buenos Aires, Argentina, in 1971. He is a Full Professor and a researcher of IITREE-LAT – a Research Institute and High Voltage Laboratory - of La Plata National University (UNLP), Buenos Aires, Argentina.

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