Predictive Direct Torque Control Using a Cascade Asymmetric Multilevel Converter

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***Abstract*— A Direct Torque Control scheme which regulates the flux and the electromagnetic torque of an induction motor (IM) is presented in this paper. A Cascade Asymmetric Multilevel Converter (CAMC) drives the IM in 7-level mode using a new voltage value for the flying capacitors. An integrated control scheme based on the Finite-Control-Set Model Predictive Control (FCS-MPC) approach undertakes the solution as a unique multi-objective control problem. The algorithm directly selects the switching states according to a rule of optimization and avoiding the use of modulators and nested controllers.**

***Keywords*— Hybrid Multilevel Converters, Predictive Control, Direct Torque Control.**

I. INTRODUCTION

Power conversion using multilevel converters is a topic of great interest since they can be connected to the medium voltage grid without a coupling transformer. They can also deliver output voltages with low harmonic content. Since the power electronic converters are a key component of modern power conditioning devices and are also essential for the integration of renewable energy sources to the grid, a lot of research is dedicated towards the improvement of converter's efficiency and control flexibility. The drawback of multilevel topologies is that they include a large number of components and interconnections that degrade system's reliability. In this sense, an intensive effort is made towards the optimization of the relationship between the number of levels and the number of switching devices (Babaei et al., 2013) (Khoucha et al., 2011). Some works address this subject and introduce arrangements of different multilevel cells with hybrid modulation schemes (León et al., 2011) or non-standard voltage progressions of converter capacitors (Lezana et al., 2009). Asymmetric structures also allow to use switches of different technologies, which may exploit more adequately their maximum switching frequency, blocking voltage and current handling capabilities. A research on increasing the ratio between number of levels and the number of switches has been introduced in (González et al., 2010). This reference presents the Cascade Asymmetric Multilevel Converter which is a low parts-count hybrid inverter with a common DC bus. The converter is operated on a simple hybrid modulation method that synthesizes the output voltage, and also maintains the balance on the flying capacitors in open loop mode. Other works use the space vector modulation technique, selective harmonic elimination (Pulikanti and Angelidis, 2011) and also predictive controllers (Geyer and Mastellone, 2012) (Kieferndorf et al., 2012) and several applications are exemplified for FACTS devices and motor drives. However in all cases, the converter synthesizes 5 levels on the output voltage with the flying capacitors charged to one fourth of the DC link voltage. Specifically, in motor drives applications, increasing the number of levels of the converter has the general advantage of current ripple reduction and concerning issues such as common mode voltages and high *dV/dt* (Naumanen et. al, 2010) (Rajeevan and Gopakumar, 2012).

In this paper, the control of torque and flux of an induction motor fed with a Cascade Asymmetric Multilevel Converter is presented. The regulation of motor variables and the internal voltages of the CAMC is addressed through a Finite-Control-Set MPC approach. A new voltage value for the flying capacitors is considered which increases the number of levels from 5 to 7 without additional components. The regulation of the flying capacitors' voltages to this non-standard value, as well as the motor variables are simultaneously achieved through the FCS-MPC scheme by direct selection of the best switching combination of the converter, without modulators and linear controllers. The evaluation of the control strategy is performed through computer simulations.

II. THE CAMC CONVERTER

One leg of the CAMC is shown in Figure 1. Its structure can be seen as a cascade connection of two stacked half-bridges, composed of transistors T1 to T4 and capacitors C_1 and C_2, and a three level flying-capacitor (FC) cell which is composed of T5 to T8 and the flying capacitor C_{fl}. The DC bus capacitors C_1 and C_2 are charged to $V_{DC}/2$ while the flying capacitor C_{fl} is usually charged to $V_{DC}/4$. In this condition the topology is able to synthesize five voltage levels at the output (v_{iN}). According to the switching signals s_1, s_2 and s_3, transistors T1 to T4 switch simultaneously and impress a voltage equal to $V_{DC}/2$ between the nodes W and Z, which constitutes the supply voltage of the flying

capacitor stage. Also, if $V_{fl}=V_{DC}/4$, there are redundant switching combinations for the synthesis of the leg voltage v_{iN}. This is, some values of v_{iN} can be obtained with more than one switching combination. Figure 2 shows the synthesis of $v_{iN}=V_{DC}/4$ and $v_{iN}=3/4V_{DC}$ which are obtained by different switching combinations. A closer look on Figure 2(a) and (b) indicates that the load current charges the flying capacitor in Figure 2(a) and discharges it in Figure 2(b), without modifying the value of v_{iN}. This is also true for Figure 2(c) and (d). Hence, if both redundant states are alternatively applied, the net charge flowing through the capacitor can be nullified maintaining a constant value for V_{fl}.

In this work, the voltage on flying capacitors $V_{fl}=V_{DC}/6$ instead of $V_{DC}/4$ is considered. The values of the leg voltage v_{iN}, for each combination of the switching functions, are listed in Table 1. Both values of the voltage V_{fl} are considered for comparison: $V_{fl}=V_{DC}/4$ and $V_{fl}=V_{DC}/6$. It is observed from Table 1 that, when $V_{DC}/4$, the switching combinations SW2 and SW3 are redundant in the sense that both states generate the same value of v_{iN} (=$V_{DC}/4$). On the other hand, when V_{fl} is $V_{DC}/6$, two different leg voltages result ($v_{iN}=V_{DC}/6$ and $V_{DC}/3$). Therefore, those redundant states are split into different voltages. Similar condition occurs with the states SW6 and SW7. The Table 1 also shows the change of the voltage values to $5/6V_{DC}$ and $2/3V_{DC}$ for SW6 and SW7, respectively. In this way, when the voltage V_{fl} is set to $V_{DC}/6$, 7 levels can be synthesized on v_{iN} with the same topology of the 5-level CAMC. It is worth mentioning that the combinations SW4 and SW5 are still redundant since both generate an output voltage equal to $V_M=V_{DC}/2$. However, this is independent of V_{fl} and both states have no incidence on the voltages of the flying capacitors.

As the leg redundancy is eliminated, the state alternation discussed from Figure 2 cannot be applied to balance the net charge on the flying capacitors.

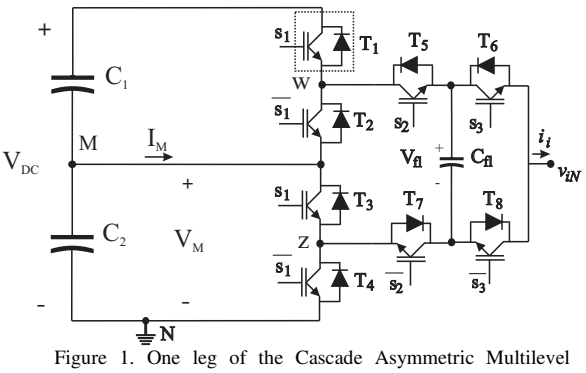

Figure 1. One leg of the Cascade Asymmetric Multilevel Converter

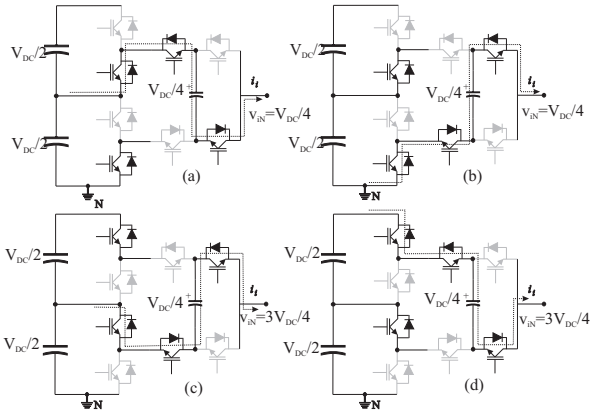

Figure 2. Redundant states of the CAMC, a), b): $v_{iN}=1/4V_{DC}$; c), d): $v_{iN}=3/4V_{DC}$.

Table 1: Voltages of the CAMC for two different values of V_{fl} and different switching combinations.

S_1	S_2	S_3	v_{iN}	$v_{iN}(V_{fl})$; ($V_M=V_{DC}/2$)		*States*
				$V_{fl}=V_{DC}/4$	$V_{fl}=V_{DC}/6$	
0	0	0	0	0	0	SW_1
0	0	1	V_{fl}	$1/4V_{DC}$	$1/6V_{DC}$	SW_2
0	1	0	V_M-V_{fl}	$1/4V_{DC}$	$1/3V_{DC}$	SW_3
0	1	1	V_M	$1/2V_{DC}$	$1/2V_{DC}$	SW_4
1	0	0	V_M	$1/2V_{DC}$	$1/2V_{DC}$	SW_5
1	0	1	V_M+V_{fl}	$3/4V_{DC}$	$2/3V_{DC}$	SW_6
1	1	0	$V_{DC}-V_{fl}$	$3/4V_{DC}$	$5/6V_{DC}$	SW_7
1	1	1	V_{DC}	V_{DC}	V_{DC}	SW_8

However, if three phase loads without neutral conductor are considered the redundancy of line voltages can assist to perform this task. This technique has been formerly used to regulate the voltages of the DC bus capacitors in diode-clamped multilevel converters (Marchesoni and Tenca, 2002). Figure 3 illustrates an example of two switching combinations that lead to the same set of line voltages. It is clear that, although the same line voltages are generated, the different paths for the line currents define different sets of voltage deviations on the three flying capacitors. Then, since the line currents only depend on the line voltages of the converter, the more adequate set of leg voltages can be evaluated to synthesize the desired line voltages while contributing to the regulation of the flying capacitors' voltages.

III. FCS-MPC CONTROLLER

Finite-Control-Set Model Predictive Control is a very interesting control strategy and has proved to be a powerful method to control power converters. The main characteristic of this technique is that it can handle the control of multiple variables of the system in a unique control formulation. This is specially useful when dealing with multilevel converters, which need some kind of control over their internal capacitors (Hu et al., 2013).

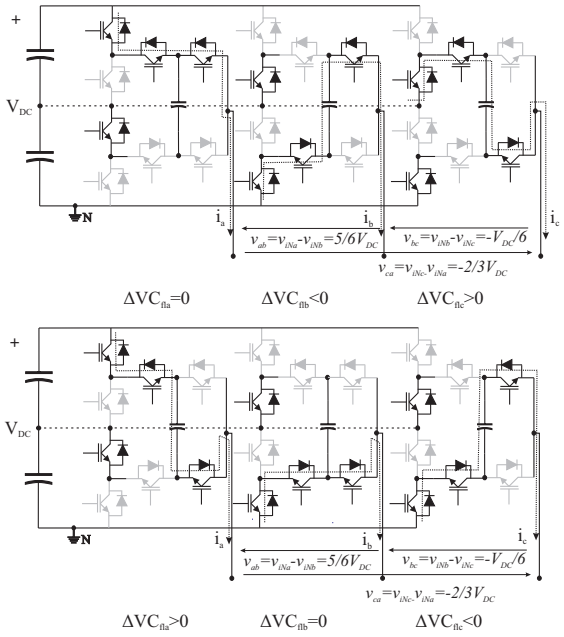

Figure 3. Two switching combinations with equal line voltages.

The method is based on setting the discrete states of the converter to suited dynamic models containing the variables of interest. The future system values are precalculated for all possible states and an optimization criterion is evaluated through a cost function of the type:

$$g(S_n) = \sum_m K_i \left| f_{mref} - f_{mpred}(S_n) \right| \quad (1)$$

where f_m are the controlled variables, S_n is the considered switching state of the three phase converter for which the predictions f_{mpred} are precalculated. The subtraction measures the difference between the reference value and the precalculated values. Each component is multiplied by a weighting-normalizing factor K_i which assigns different emphasis to each control variable. In this work, the joint control of the CAMC and an induction motor through FCS-MPC operating in 7-levels mode is analyzed. For simplicity, two groups of controlled variables are defined: the external variables, which are the primary control targets and also the converter variables, which are necessary to safely operate the converter with 7 levels. The machine cost function takes into account the torque and the stator flux:

$$g_{ext} = K_T \cdot g_T + K_\psi \cdot g_\psi \quad (2)$$

where g_T and g_ψ are the corresponding torque and flux cost functions and K_T and K_ψ are their respective weighting factors. On the other hand, the internal converter variables are the voltages on the three flying capacitors and also the midpoint voltage of the DC bus. This is essential in order to prevent overvoltage on the power switches and also to ensure equal amplitude of the voltage steps at the output. Similarly to g_{ext}, the cost fuction g_{int} is:

$$g_{\text{int}} = K_{fl} \cdot g_{fl} + K_M \cdot g_M \quad (3)$$

Here, g_{fl} is the cost function associated with the voltage on the flying capacitors and g_M is associated with the voltage of the midpoint of the DC bus. K_{fl} and K_M are their respective weighting factors. The switching state is selected by merging both control targets in a unique cost function g:

$$g = g_{ext} + g_{\text{int}} \quad (4)$$

All candidate switching states are directly evaluated through g and the one that minimizes it is selected for application in the next sampling interval.

A flow diagram of the proposed algorithm is shown Figure 4. The process begins with the generation of the set of possible switching states S_1 to S_j from the current state S[k]. Each state is set as the input to the dynamic model of the system and one step forward calculation is performed to generate the predicted outputs. These values are incorporated to the cost function g, jointly with the references, and the switching combination that minimizes g is selected as the next state of the converter.

A. CAMC model

Flying capacitors voltage term

The voltage deviation on each flying capacitor is uniquely defined by the path of the phase current. The Table 1 shows that only for the states SW_2, SW_3, SW_6 and SW_7, the phase current flows through the flying capacitor, and thus, a voltage deviation is produced. Moreover, taking into account the selected direction of current flow, SW_3 and SW_7 generate a charging effect on C_{fl} while SW_2 and SW_6 discharges it. On the other hand, SW_1, SW_4, SW_5 and SW_8 do not have any effect, provided that the current does not flow through C_{fl}. Figure 5 shows a flowchart which determines the voltage deviation of C_{fl}, by virtue of the above discussion, and considering that the current is constant along the sampling period T_S. This structure is evaluated for C_{fla}, C_{flb} and C_{flc}. At instant k the voltages on the flying capacitors are sampled. The precalculation of the voltage deviations on the flying capacitors allows one to obtain an estimation at the next sampling instant for the considered switching combinations. Then, the goodness of each switching combination can be evaluated by a cost function g_{fl} (5) which measures the mean relative error between the predicted voltages and the reference voltage.

$$g_{fl} = \frac{1}{3V_{fl\_ref}} \sum_{i=a,b,c} \left| V_{fl\_ref} - (V_{Cfli}[k] + \Delta VC_{fli}) \right| \quad (5)$$

Here, V_{fl_ref} is the reference voltage, V_{Cfli}[k] is the sampled value, and ΔVC_{fli} is the voltage deviation of capacitor i calculated with the flowchart of Figure 5.

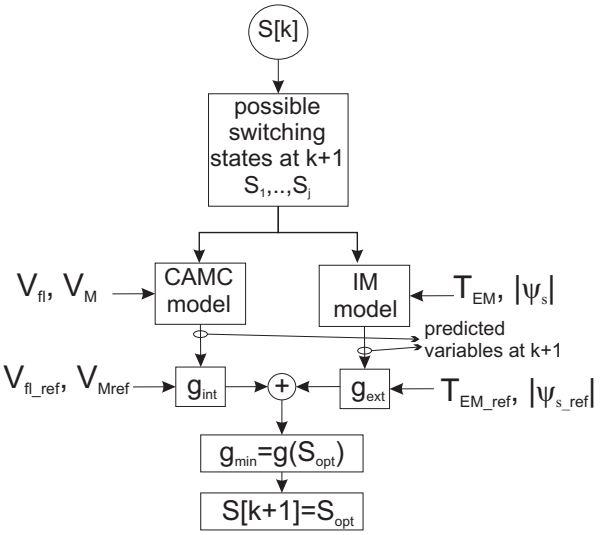

Figure 4. Flow diagram of controller calculations

DC bus balance term

In the case where the DC bus is fed with a single voltage source V_{DC}, the voltage of the node M with respect to the negative of the DC bus is not fixed and may suffer from fluctuations or even continous voltage drift. Then, a control effort is directed to maintain the voltage of node M to $V_{DC}/2$. In order to determine how each switching state affects the voltage balance of the DC bus, a simple calculation of the voltage deviation of V_M can be performed.

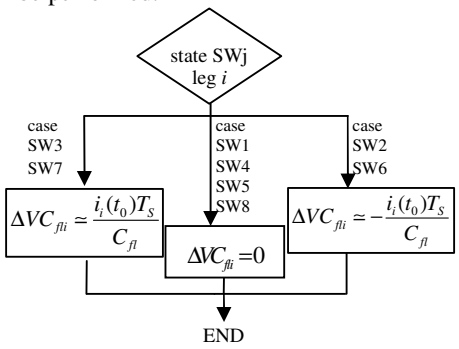

Figure 5. Flowchart for the calculation of voltage deviations on the flying capacitors.

Looking at Table 1 and with the help of Figure 6 it is easy to see that the switching combinations SW1,2,7 and 8 do not affect V_M, since V_M is not involved in the expression of the output voltage. On the contrary, SW3,4,5 and 6 imply that the phase current is drawn from/to the M node (Figure 6). Therefore, considering C_1=C_2=C and for slow current variations along the sampling period, the voltage deviation ΔV_M due to the current of leg i (i=a,b,c) can be calculated following the flowchart of Figure 7.

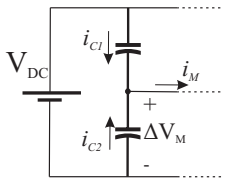

Figure 6. Voltage deviation on the midpoint of the DC bus

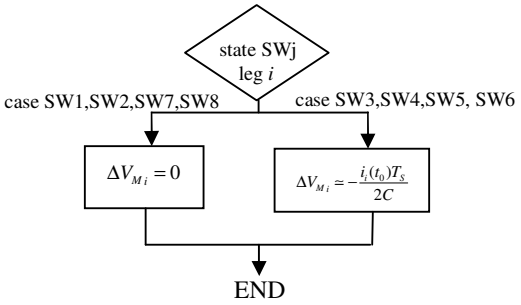

Figure 7. Calculation of voltage deviation on the midpoint of the DC bus.

The contributions to the voltage deviation of node M due to the three phase currents (i=a,b,c) are summed up to give the net contribution ΔV_{MT}. In order to measure the voltage balancing condition, the function g_M calculates the relative error between $V_{DC}/2$ and the calculated value of V_M.

$$g_M = \frac{\left| V_{DC}/2 - (V_M[k] + \Delta V_{MT}) \right|}{V_{DC}/2} \tag{6}$$

B. Induction motor model

The calculation of the predicted values of flux and torque is accomplished starting from the representation of the IM as developed in (Holtz, 1995). This work describes the dynamics of the stator current and magnetic flux of the machine:

$$\begin{cases} \dfrac{d\boldsymbol{\psi}_s}{dt} = \mathbf{V}_s - r_s \mathbf{i}_s & \text{(a)} \\ \tau'_{sr}\dfrac{d\mathbf{i}_s}{dt} + \mathbf{i}_s = j\omega_r \tau'_{sr}\mathbf{i}_s + \dfrac{1}{r_{sr}}\left(\dfrac{1}{\tau_r} - j\omega_r\right)\boldsymbol{\psi}_s + \dfrac{1}{r_{sr}}\mathbf{V}_s & \text{(b)} \end{cases} \tag{7}$$

$$k_s = \frac{L_m}{L_s},\ k_r = \frac{L_m}{L_r}, \sigma = 1 - k_s k_r,\ \tau_r = \frac{L_r}{r_r}, r_{sr} = r_s + \frac{L_s}{L_r} r_r, \tau'_{sr} = \frac{\sigma L_s}{r_{sr}}$$

where: $\mathbf{V}_s$: *stator voltage*
$\mathbf{i}_s$: *stator current*
$\boldsymbol{\psi}_s$: *stator flux*
ω_r: *rotor frequency*
L_m: *magnetizing inductance*
L_s: *stator inductance*
L_r: *rotor inductance*
r_r: *rotor resistance*
r_s: *stator resistance*

Discretizing (7) with the Euler approximation and solving for current and flux at the instant $k+1$ yields to:

$$\begin{cases} \boldsymbol{\psi}_s[k+1] = (\mathbf{V}_s[k] - r_s \mathbf{i}_s[k]) T_S + \boldsymbol{\psi}_s[k] \\ \mathbf{i}_s[k+1] = \left(\mathbf{i}_s[k] \left(\frac{\tau'_{sr} - T_S}{\tau'_{sr}} + j\omega_r T_S \right) \right) + \frac{T_S}{\tau'_{sr} r_{sr}} \left(\frac{1}{\tau_r} - j\omega_r \right) \boldsymbol{\psi}_s[k] + \frac{T_S}{\tau'_{sr} r_{sr}} \mathbf{V}_s[k] \end{cases} \quad (8)$$

The EM torque of the machine can be calculated in terms of the real and imaginary components of flux and current at instant $k+1$ according to:

$$T_{EM}[k+1] = \frac{3}{2} p \left(\psi_{s\alpha}[k+1] i_{s\beta}[k+1] - \psi_{s\beta}[k+1] i_{s\alpha}[k+1] \right) \quad (9)$$

The predictions of flux and torque for the different switching states $\mathbf{V}_s$ are compared through (10).

$$g_\psi = \frac{\left| \psi_{ref} - |\boldsymbol{\psi}_s| \right|}{\psi_{ref}} \quad \text{and} \quad g_T = \left| \frac{T_{ref} - T_{EM}}{T_{ref}} \right| \quad (10)$$

Once (5), (6), and (10) are calculated, the cost functions (2) and (3) and finally (4) is computed for the considered set of switching states, and the switching state that minimizes g is selected for the next sampling period.

IV. PERFORMANCE EVALUATION

The control algorithm is evaluated by means of computer simulations. The test proposal consists on two sets of results in which the regulation of internal and external variables is analyzed. The first test shows the ability of the controller to regulate the internal voltages of the converter with the IM operating at rated speed and torque. The second test evaluates the dynamic response of the EM torque and the flux when a sudden change of the torque reference signal is produced. A block diagram of the test setup is shown in Figure 8, and the system parameters are specified in Table 2.

A. Control of the internal voltages of the CAMC

A first test is performed to verify the effectiveness of the controller to regulate the voltages on the internal capacitors of the CAMC. For this, a voltage unbalance is simultaneously forced by external means on the flying capacitors and in the midpoint of the DC bus. A 10% voltage deviation is imposed in *t=5.6s* on the flying capacitors and in V_M. Figure 9(a) shows the voltage on the midpoint of the DC bus which is *5.7kV*.

Table 2. System parameters

Motor Parameters					
Rr	**Llr**	**Rs**	**Lls**	**Lm**	**U_{nom}**
0.56Ω	23mH	1.26Ω	42mH	0.3H	6.6kV
I_{nom}	**PF**	**poles**	**f**	**T_{nom}**	**Inertia**
120A	0.87	4	50Hz	6.4kNm	11kgm^2
CAMC Parameters					
	V_{DC}	**C_{fl}**	**C_1, C_2**	**T_S**	
	11.5kV	1.5mF	1.5mF	0.1ms	

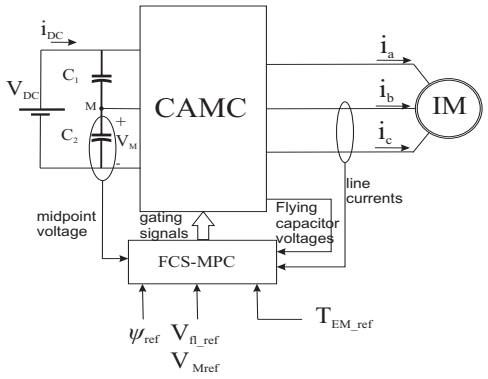

Figure 8. Test setup of the IM drive using the CAMC converter.

Figure 9(b) shows the voltages on the three flying capacitors which have a nominal value of *1.9kV=V_{DC}/6*. It can be observed that whilst the voltage on the midpoint of the DC bus needs almost *400ms* to recover the setpoint value, the three flying capacitors yield it in approximately *100ms*. Also, a detail of the voltage ripple on the flying capacitors is seen on Figure 9(c), which is near 50V_{pp} (2.5%).

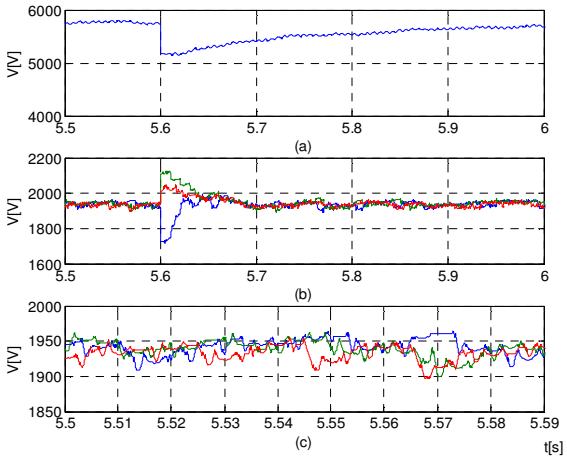

Figure 9. Forced unbalance on the flying capacitors and on the midpoint of the DC bus (T_L=2400Nm, n=1490RPM). a) V_M, b) Voltage on the flying capacitors, c) Detail of voltage ripple on the flying capacitors.

B. Step variation on the EM torque command signal without speed regulator

In this test, the system operates close to nominal regime and the EM torque setpoint is suddenly changed. The torque signal is initially set (*t<4s*) to positive (motoring) value of *2400Nm*. It is suddenly changed to a rated breaking torque of *6400Nm* (*4<t<4.05s*) and is turned back to positive with rated value. Figure 10(a) shows the reference command (black) and the estimated EM torque (light gray). A detail of Figure 10(a) shows a torque settling time of approximately 3*ms* while the peak can be estimated to *250Nm*. The quadrature components of IM flux and the line currents are shown

in Figure 10(b) and (c), respectively. All waveforms have sinusoidal shape while the currents exhibit a small high frequency ripple and feature rapid amplitude and phase transitions at the instants of torque reference variation. Figure 10(d) shows one line voltage. It can be observed that the converter synthezises 13 voltage levels on the line voltage in contrast with the 9 levels which are obtainable when $V_{fl}=V_{DC}/4$. Also, the voltage mostly varies in single steps, which effectively reduces the *dV/dt* on motor terminals.

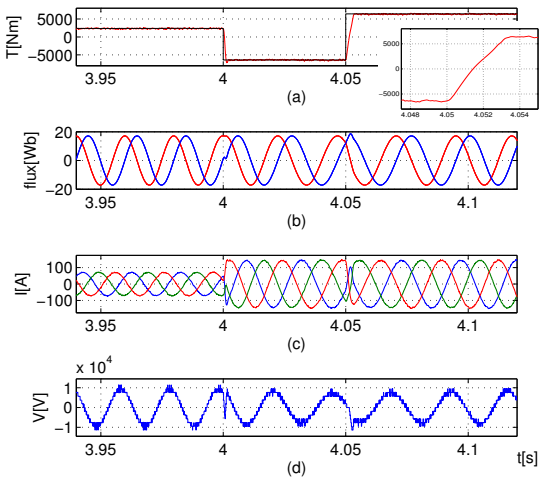

Figure 10. Step variation of the torque reference input of the MPC controller. a) Reference torque (black) and EM torque (gray), b) Motor currents, c) Motor voltage, d) Detail of motor voltage.

V. CONCLUSIONS

This paper presents and induction motor drive scheme using a Cascade Asymmetric Multilevel Converter. The control strategy of the entire system includes the motor variables and internal voltages of the converter and is based on a Finite-Control-Set Model Predictive Control approach. The controller regulates the voltages on the flying capacitors and the DC link capacitors to maintain the internal voltage balance and the stator flux of the machine, and simultaneously performs the tracking of the electromagnetic torque reference signal. An analysis of the voltage value of the flying capacitors is made from which it follows that the number of levels can be increased if the redundant states of the converter are eliminated. A particular value is chosen which adds 2 levels (to the existing 5) to the topology without additional switches and thus improving the quality of the output voltage.

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