JCS&T Vol. 11 No. 1 April 2011

Book Review:

Diseño y evaluación de arquitecturas de computadoras Marta BERTRÁN PARDO y Antonio GUZMÁN SACRISTÄN PEARSON EDUCACIÓN, S.A., Madrid, 2010 ISBN 978-84-8322-650-6

In the first paragraph of the Introduction of the book the authors say "The definition of computer architecture has generated many discussions since the emergence of what could be considered the first computer in 1943, the ENIAC". Later they add "The main idea of all the proposals made in this direction is the same: define of computer components in different levels of study to produce a hierarchical description and to facilitate their understanding and design".

The authors' goal is to provide a textbook (written in Spanish) that systematically collect the most important techniques of design and evaluation of computer architectures.

The approach is purely didactic which incorporates numerous illustrative figures and worked examples, summaries of important concepts, suggested exercises and self-evaluations as well as bibliography and suggested reading.

Throughout the book is used the architecture of a RISC processor, called nanoMIPS, based on the same principles of design of MIPS, SPARC and PowerPC

The authors organize the book in six chapters. Each chapter has a precise and well-done introduction, describing the evolution of the topic, the relationships with previous chapters or necessary previous knowledges and in some of them, updated practical cases are detailed. .

Chapter 1 – Basic Concepts of Processors – is related to the basics concepts of the design of RISC instructions sets, the pipeline (it's motivation, performance, limitations, etc), the design techniques of pipelined processors with one or more funtional units, alternatives to solve hazards on those processors and exceptions treatments techniques. Also differents data paths are shown.

Chapter 2 – Basic Concepts of Memory and I/O - shows and justified the need of a memory hierarchy in modern computers architectures. Designs topics about each level of hierarchy are despicted. The I/O system is developed based on the three main aspects that influence the performance: interconnection buses, I/O devices and I/O tasks. Although design of I/O devices are not in the scope of the book, the design of bus hierarchy and I/O manegement procedures are described.

Chapter 3 – Techniques for increased performance for processors - explores tools and techniques to optimize the risc processor designed in chapter 1. Beginning with dynamic techniques to solve data and control hazards in pipelined processors, dynamic schedule of instruction execution and dynamic branch prediction, the way to minimize stalls in data paths are presented. Instruction level paralelism are used to improve the performance. Also, multiple emission of instructions, speculative execution and multithreading solutions are presented.

Chapter 4 - Techniques for increased performance for memory and I/O - presents design techniques for cache and main memory to allow leverage of the memory hierarchy of a system, which applied to a basic memory as presented in Chapter 2, get the desired performance for architecture. They also present optimization techniques to I/O system based on three groups: those that improve the performance of the buses included in this system, those that improve the performance of the I/O devices and those that optimize I/O system management.

Chapter 5 - Multiprocessor and Multicomputer systems - begin with a classification of architectures composed of multiple processors, depending on its memory model (shared or distributed). Then, the authors present the basics of networking within computer architectures, since aspects of its design can have a major influence on overall system performance. Finally, the autors examine techniques and design decisions associated with shared memory

JCS&T Vol. 11 No. 1 April 2011

architectures (multiprocessors) and distributed memory architecture (multicomputers).

Chapter 6 - Performance evaluation - outlines the basics of performance evaluation of computer architectures. Provides guidelines and recommendations for choosing appropriate performance metrics and define simple metrics that can be used in general contexts of evaluation. Amdhal and Gustafson laws are introduced and used in different scenarios to compare and interpret results of the metrics..

This book is especially appropriate for those (teachers and students) involved with tipical contents of computer architecture with a complete and balanced view of the topic. Chapters 1 and 2 provide a basic understanding of processors while the rest of the book gives deeper explanations of what a modern processor have in it and how we can compare or evaluate performance..

Horacio A. Villagarcía Wanza hvw@info.unlp.edu.ar